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**Figure 10-1. Routing Illustration for PROCHOT# Topology**

The diagram illustrates the PROCHOT# topology. A horizontal chain of components is shown, starting from a voltage source  $V_{DDST}$  connected to a resistor  $R_{\text{unstuff}}$  (labeled "Hysteresis"). This is followed by a series of microprocessors  $M_0, M_1, M_2, M_3, M_4, M_5, M_6$ . Below  $M_0$  is "Agent 1" connected via resistor  $R_1$ . Below  $M_1$  is "Agent 2" connected via resistor  $R_2$ . Below  $M_2$  is "Agent 3" connected via resistor  $R_3$ . Below  $M_3$  is "Agent 4" connected via resistor  $R_4$ . Below  $M_4$  is "Agent 5" connected via resistor  $R_5$ . Below  $M_5$  is an "Inv OD" block connected via resistor  $R_6$ , which is further connected to a block labeled  $N_0$  and then to a block labeled "EC". Below  $M_6$  is a resistor  $R_7$  connected to a voltage source  $V_{DDSTG}$ . A resistor  $R_8$  is connected between  $M_6$  and  $M_{CPU}$ . The chain ends with  $M_{CPU}$  connected to a "CPU" block. Calculations for total resistance are provided:  $200 \text{ ohm} = R_1 + R_{\text{Agent}} = 75 \text{ ohm}$  (for Agent 1),  $200 \text{ ohm} = R_4 + R_{\text{Agent}} = 75 \text{ ohm}$  (for Agent 4), and  $200 \text{ ohm} = R_6 + R_{\text{Inv OD}} = 75 \text{ ohm}$  (for the Inv OD block). Specific resistor values are also noted:  $R_{\text{unstuff}} = 1 \text{ Kohm}$  and  $R_8 = 500 \text{ ohm}$ .

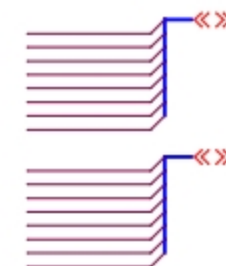
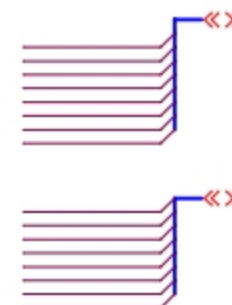
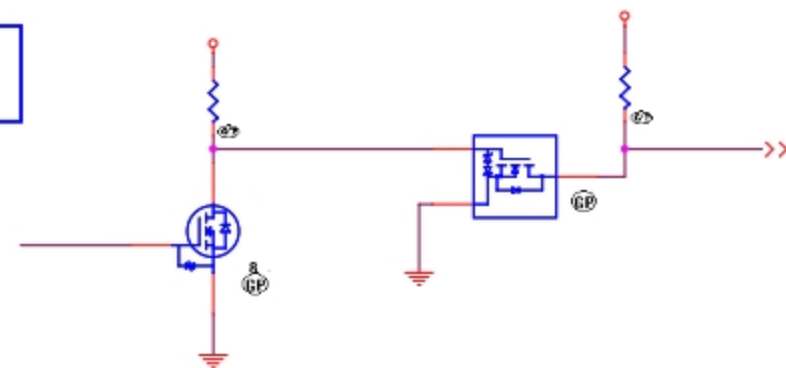


#### 4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

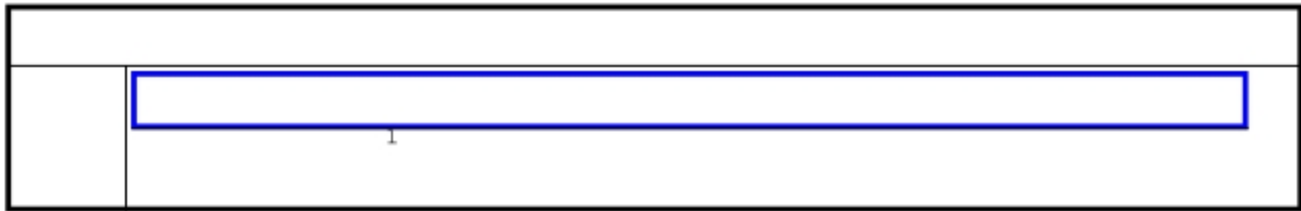
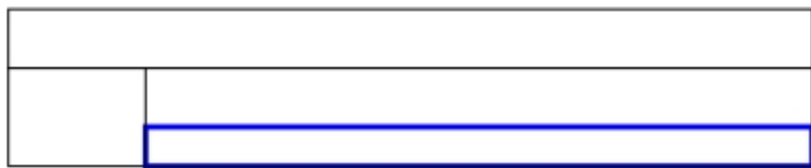
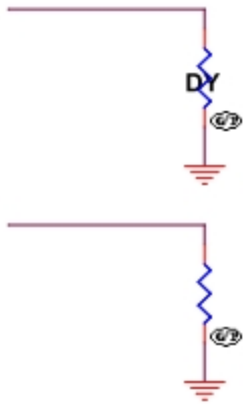
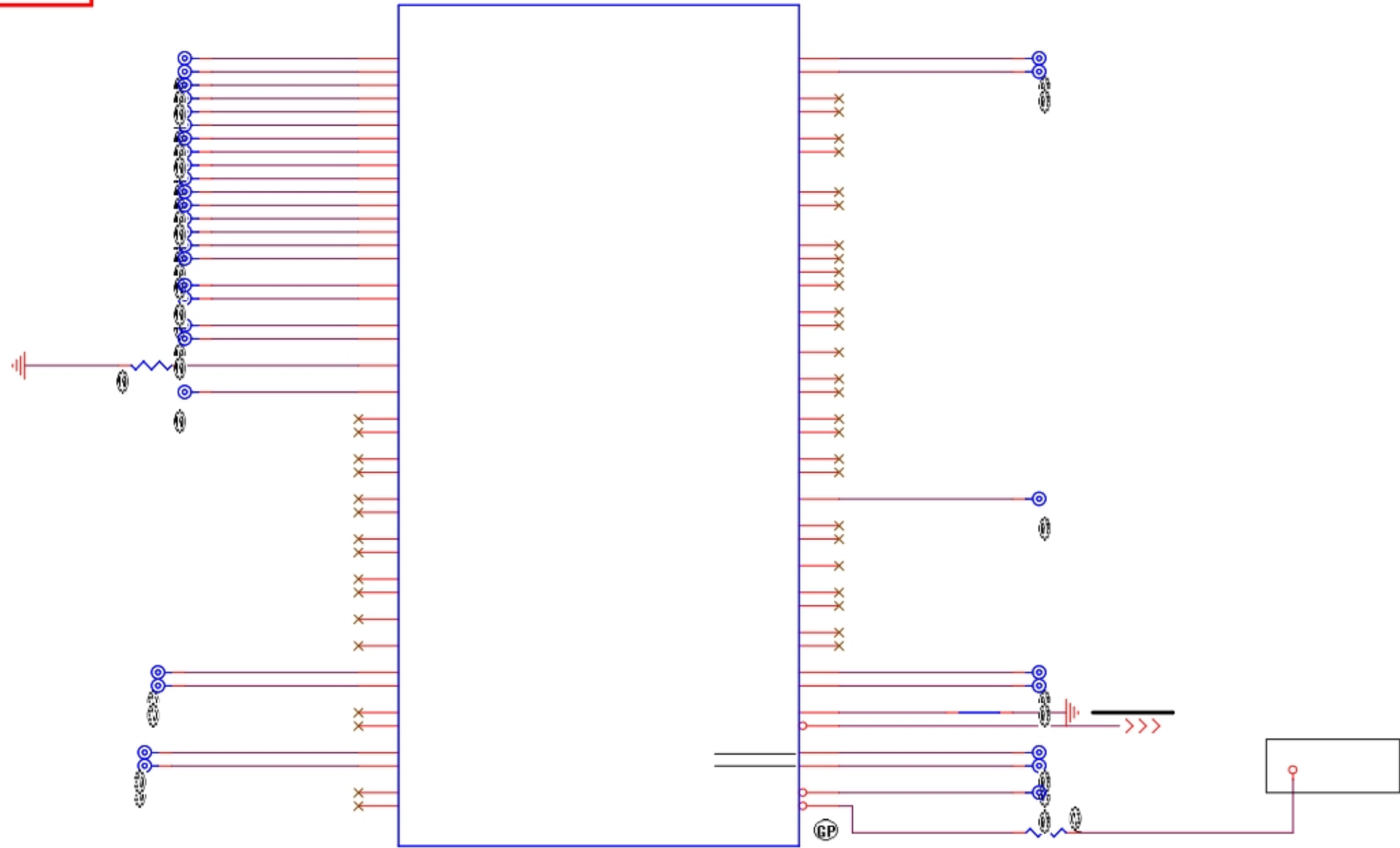
Table 4-41. ODT Signals Connectivity table

Processor	Memory Type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processor	DDR0_ODT[0]	Processor's ODT[0] connected to DRAM's ODT1. Topology connection.	1,2
SKL-U	LPDDR3 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAM's ODT1. Topology connection. Processor's ODT[1] not connected.	1,2
DDR3L Memory Down	Processor	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAM's Rank0 ODT. Processor's ODT[1] connected to DRAM's Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	2,4
DDR3L SO-DIMM	DIMM	DIMM	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] connected to DIMM's ODT[1:0].	1,2
DDR3L Mixed Memory Down and SO-DIMM	DIMM	DIMM	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DIMM's Rank0 ODT. Processor's ODT[1] connected to DIMM's Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	1,2
DDR4 Memory Down	Processor	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAM's Rank0 ODT. Processor's ODT[1] connected to DRAM's Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	
DDR4 SO-DIMM	DIMM	DIMM	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] both connected to DIMM's ODT[1:0] both.	

Notes:  
1. For additional ODT signal connection details, reference the Customer Reference Board (CRB) schematics and board files (VVP2 - SKL-U LPDDR3, VVP3 - SKL-U LPDDR3, VVP4 - SKL-U LPDDR3).  
2. LPDDR3 Rank0 ODT is always disabled by BIOS/PMC. ODT signal is controlling only Rank0 ODT.  
3. DDR3L ODT input is held high (Active). ODT signal is defined by BIOS as high-2 in both ranks, when a Rank receives write command it enables R0 ODT (for R0 side) and R1 ODT (for R1 side). ODT signal is high-2 in both ranks.  
4. These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DOP single side, 2R x16 ROP dual side and 2R x8 dual side.



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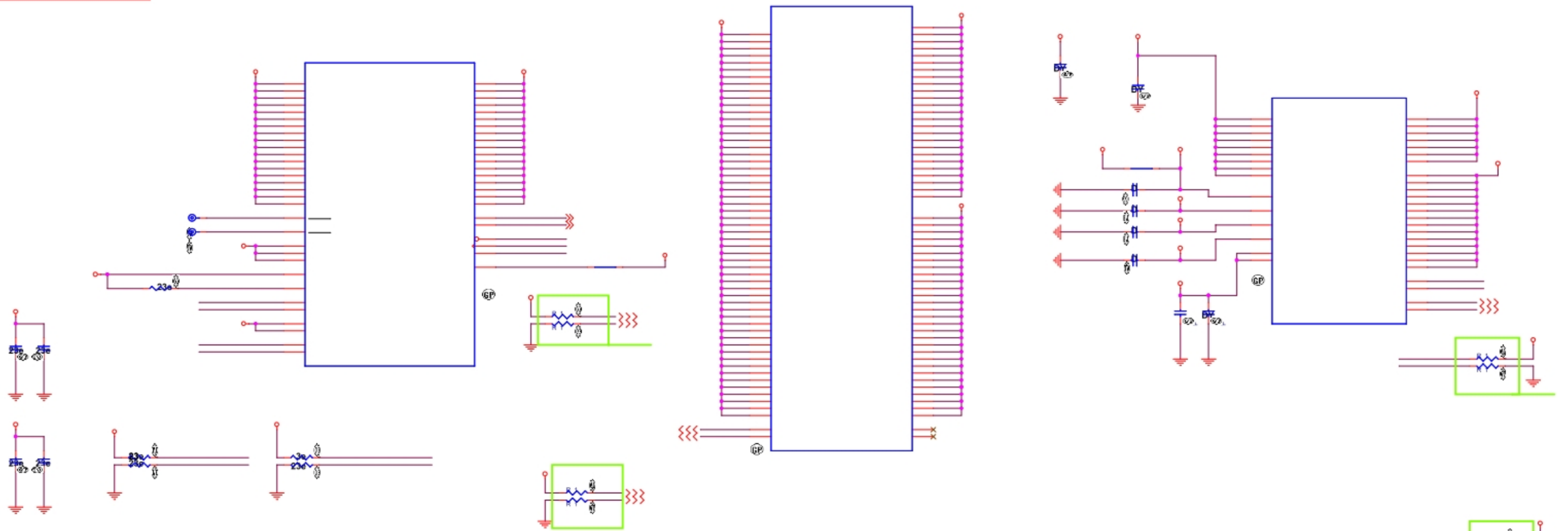
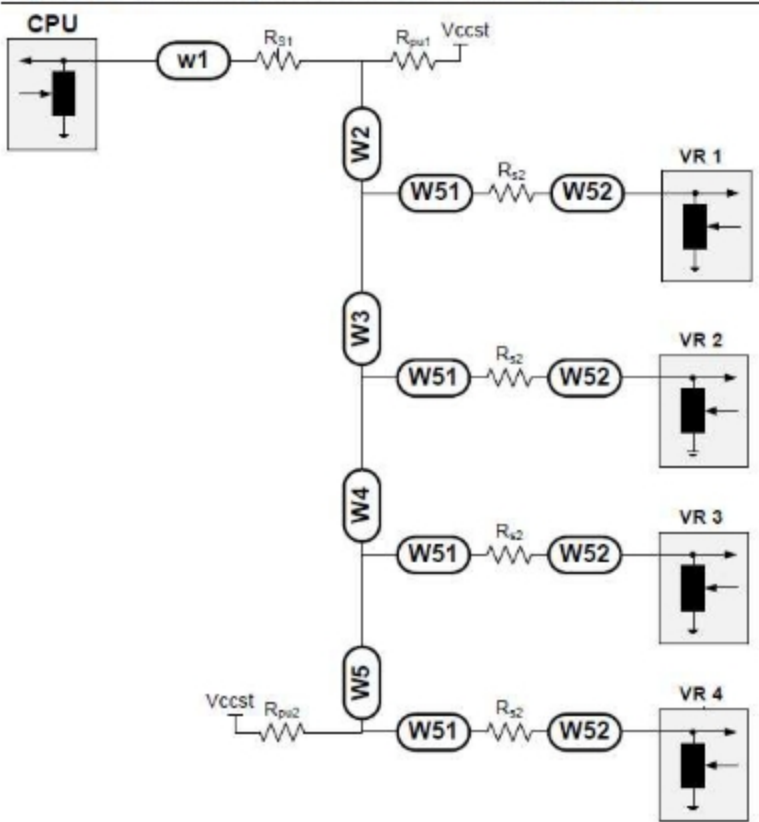
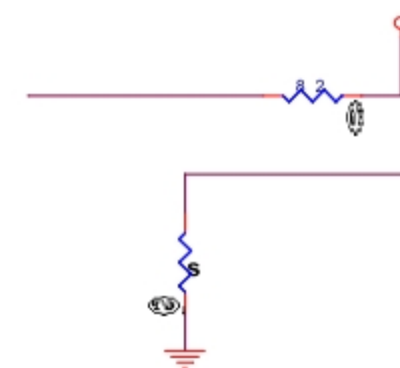
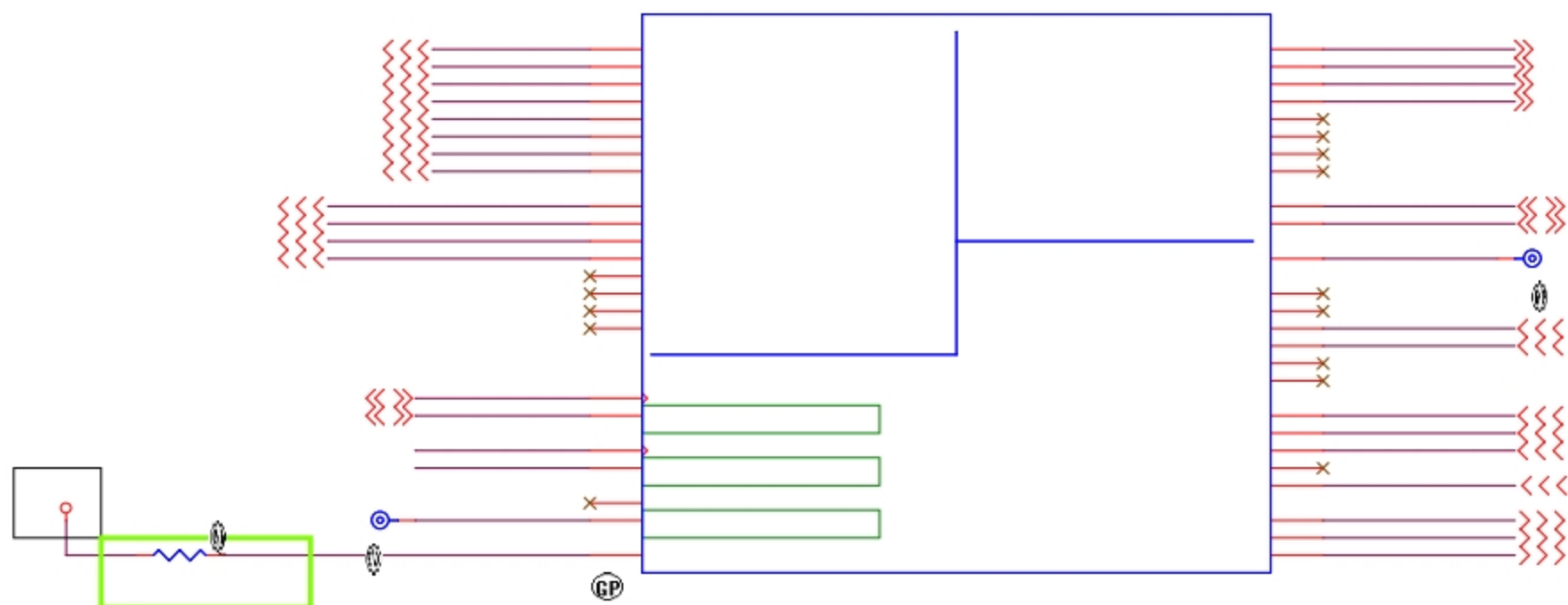
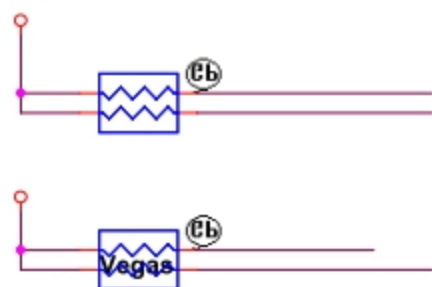


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R <sub>pu1</sub> [Ω]	R <sub>pu2</sub> [Ω]	R <sub>s1</sub> [Ω]	R <sub>s2</sub> [Ω]	V <sub>CCST</sub> [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

Figure 10-7. Routing Illustration for SVID Topology








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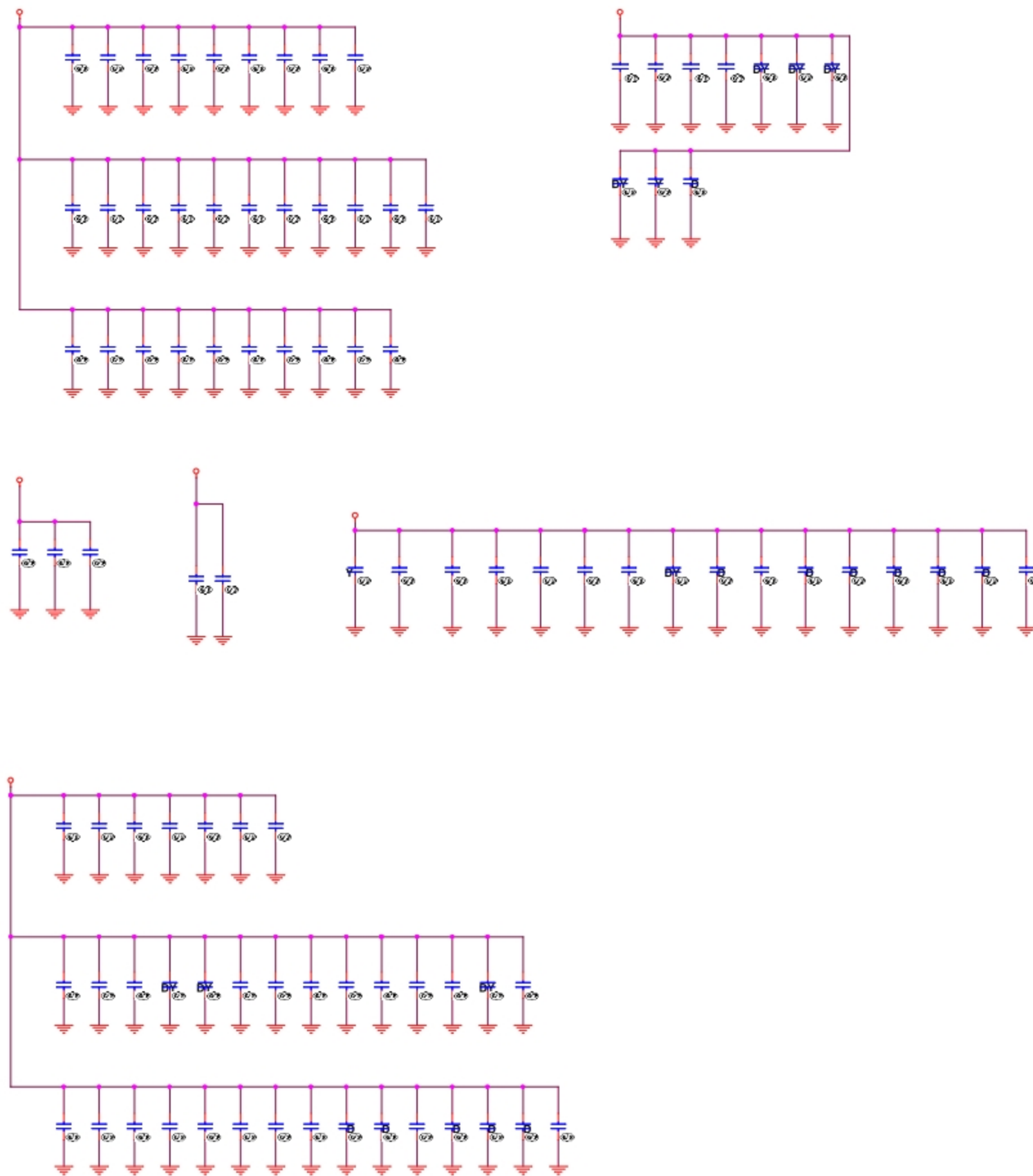


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mΩ ESR)	Placed at primary side near to VR output
VCCGT Power Plane at VR output	1x 220uF (@4.5mΩ ESR)	Placed at backside side near to VR output
VCCGTx Power Plane at VR output	2x 220uF (@4.5mΩ ESR)	Placed at primary side near to VR output
VCCIO Power Plane at VR output	1x 220uF (@4.5mΩ ESR)	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Additional components needed when supporting 23e
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

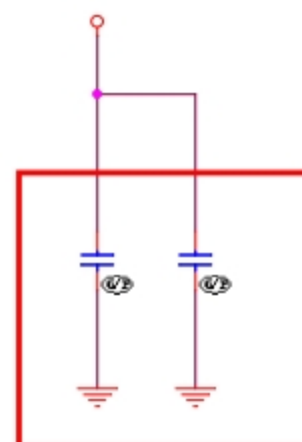
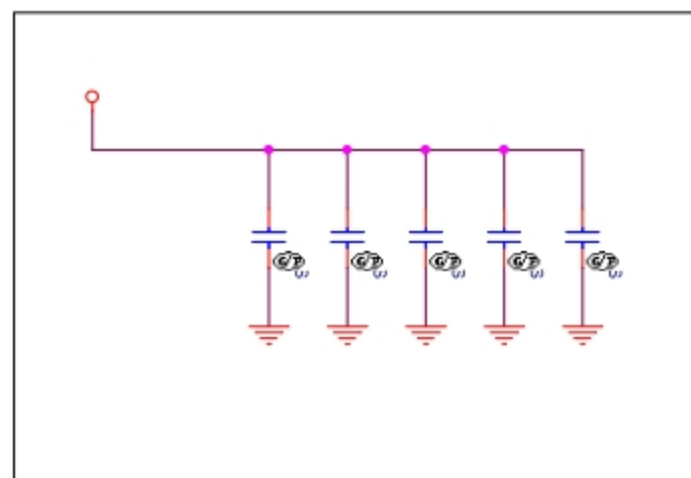
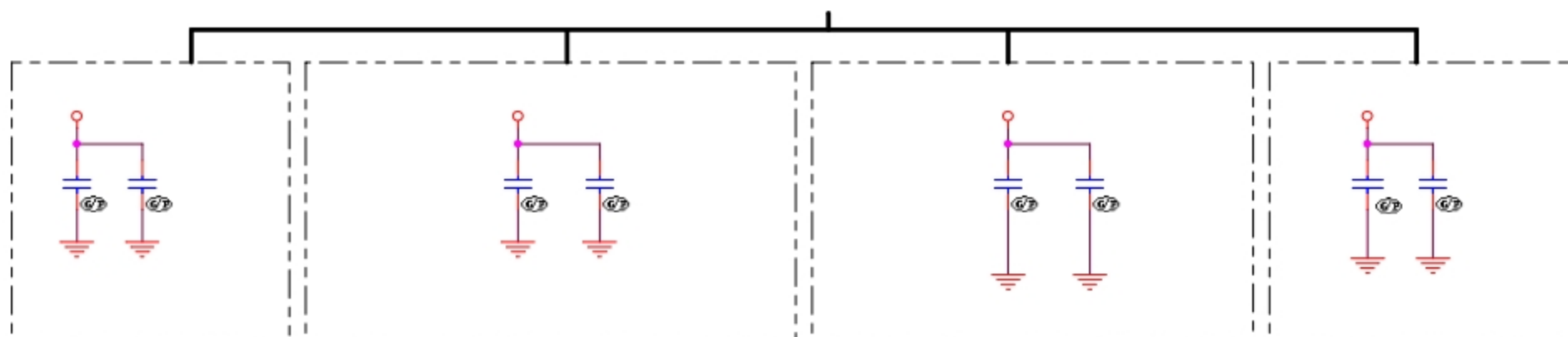
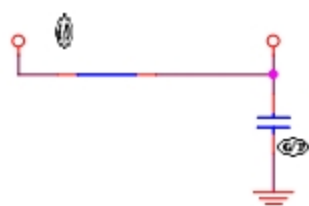
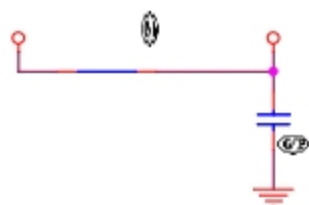
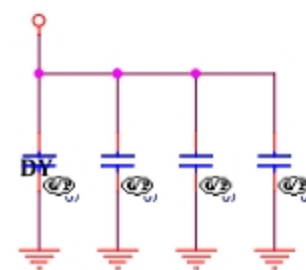
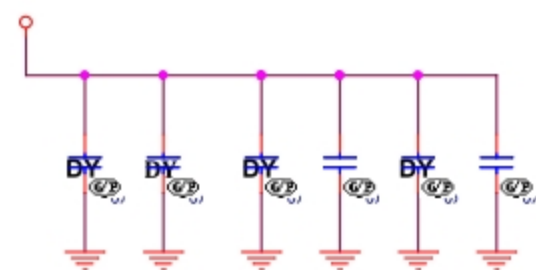
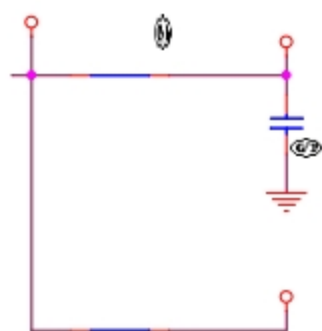
Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

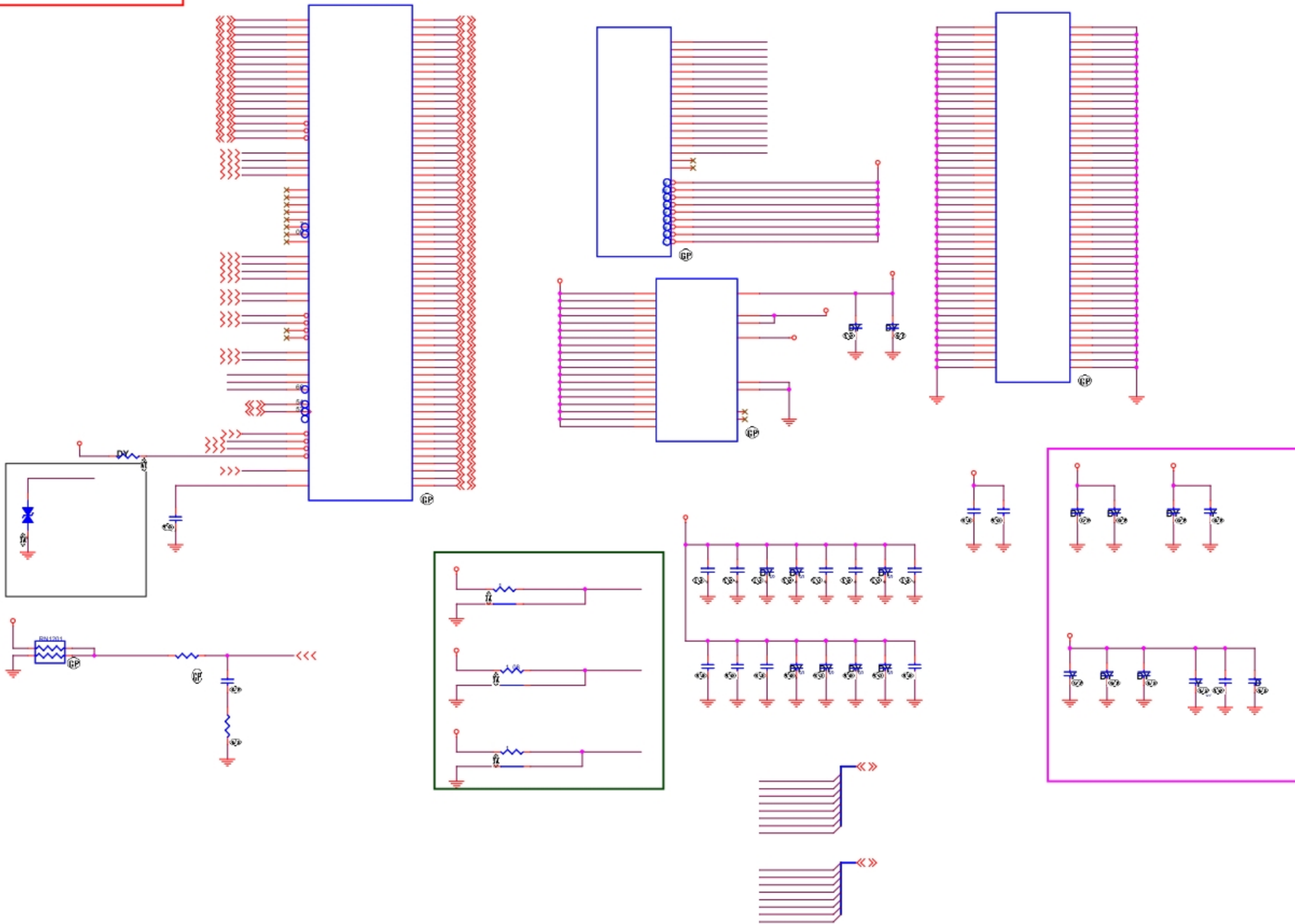
Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V) <sup>1</sup>	Place as close to the package as possible
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V) <sup>1</sup>	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible
		5x 22uF 0603	Additional components needed when supporting 23e
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package
VCCSTG			Placeholder only
VCCSTG	2x 10uF 0402		Place on secondary side, underneath the package
VCCSTG	1x 10uF 0402		Place on secondary side, underneath the package
VCCSTG	6x 1uF 0201		

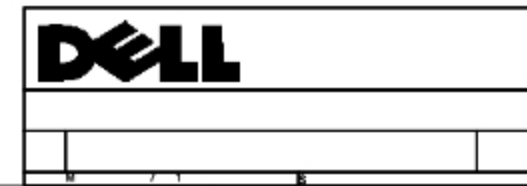






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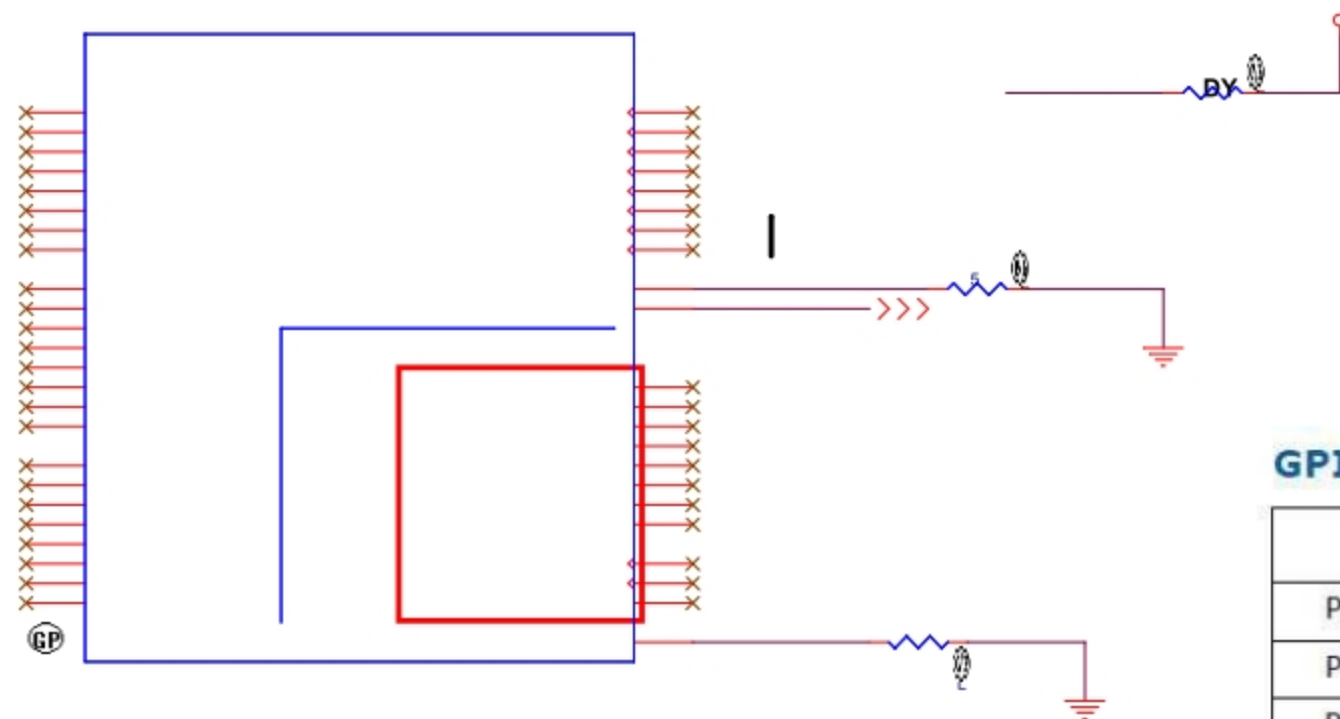


Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSENT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

## GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

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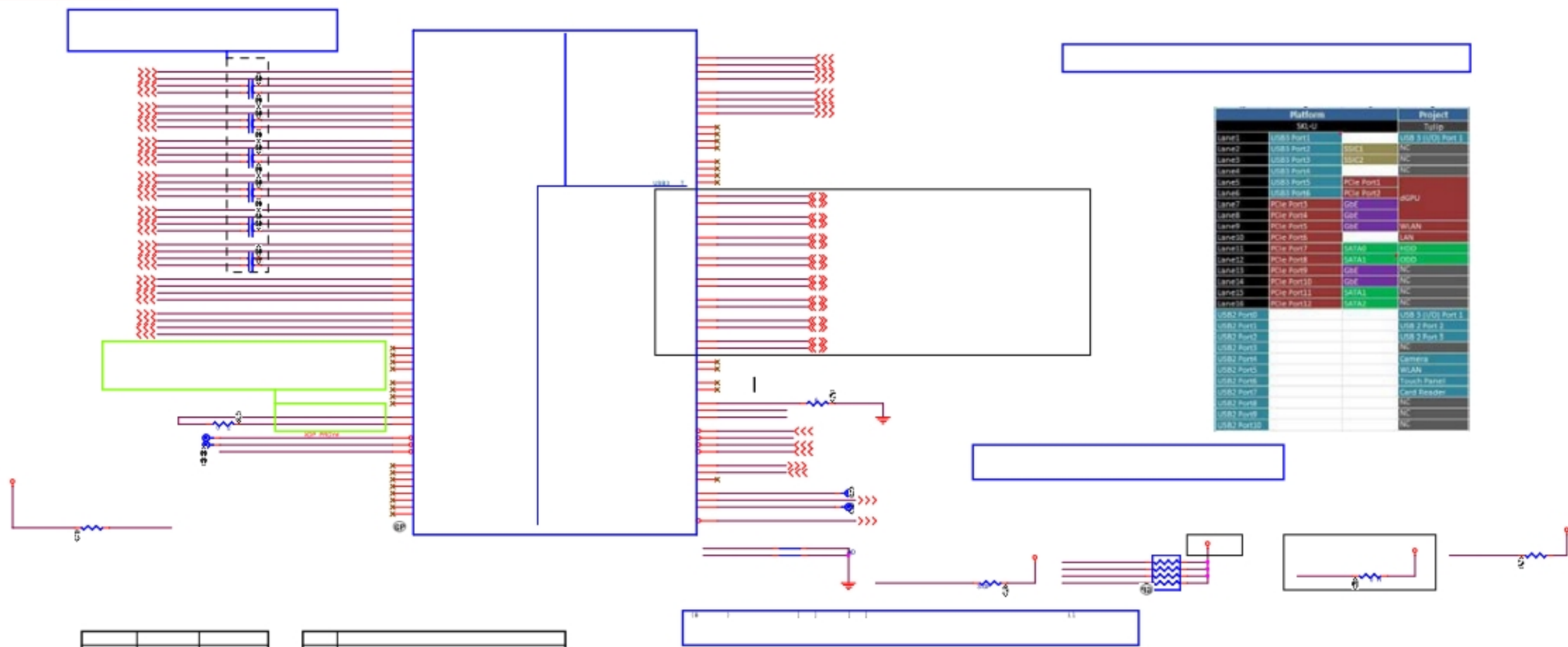


Table 24-2. PCI Express® Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe® Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

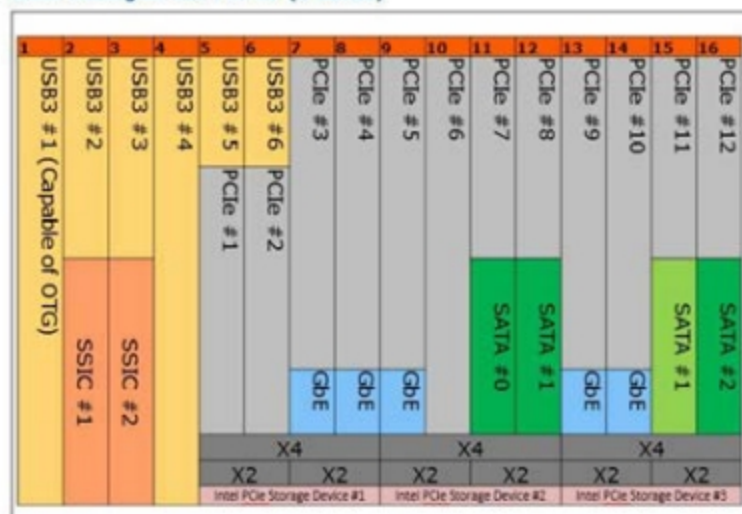
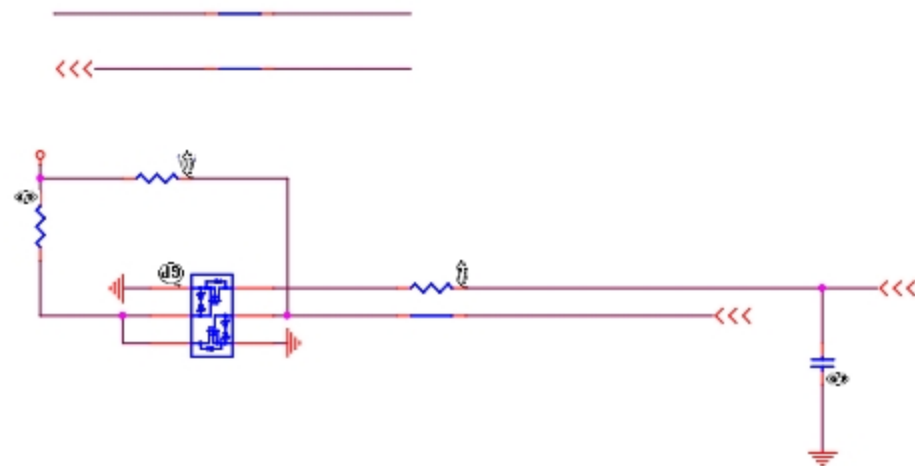
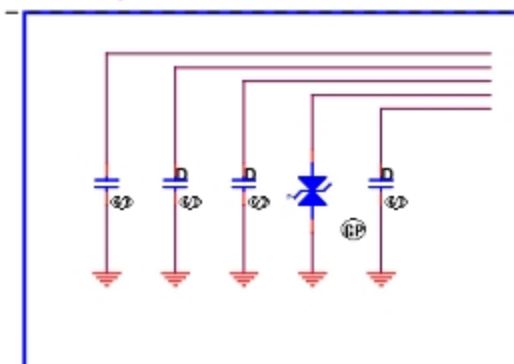
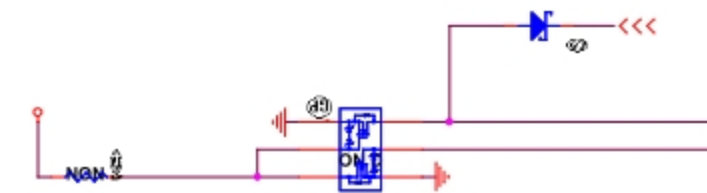
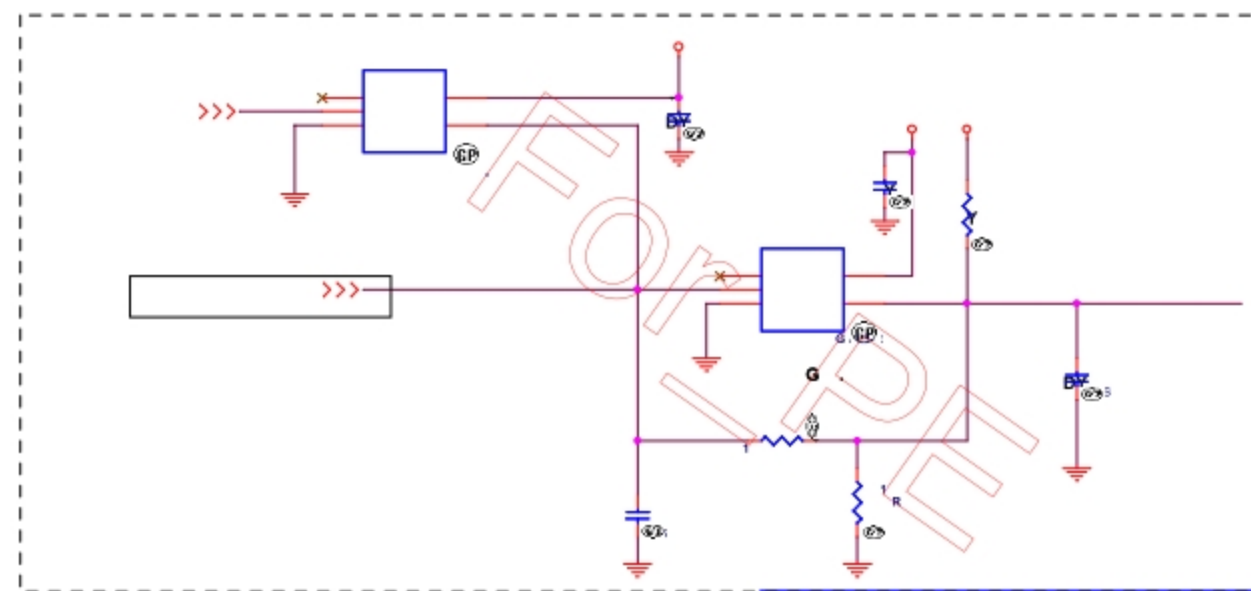
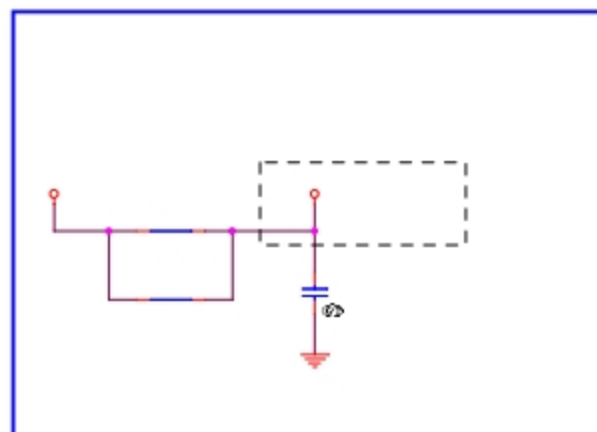
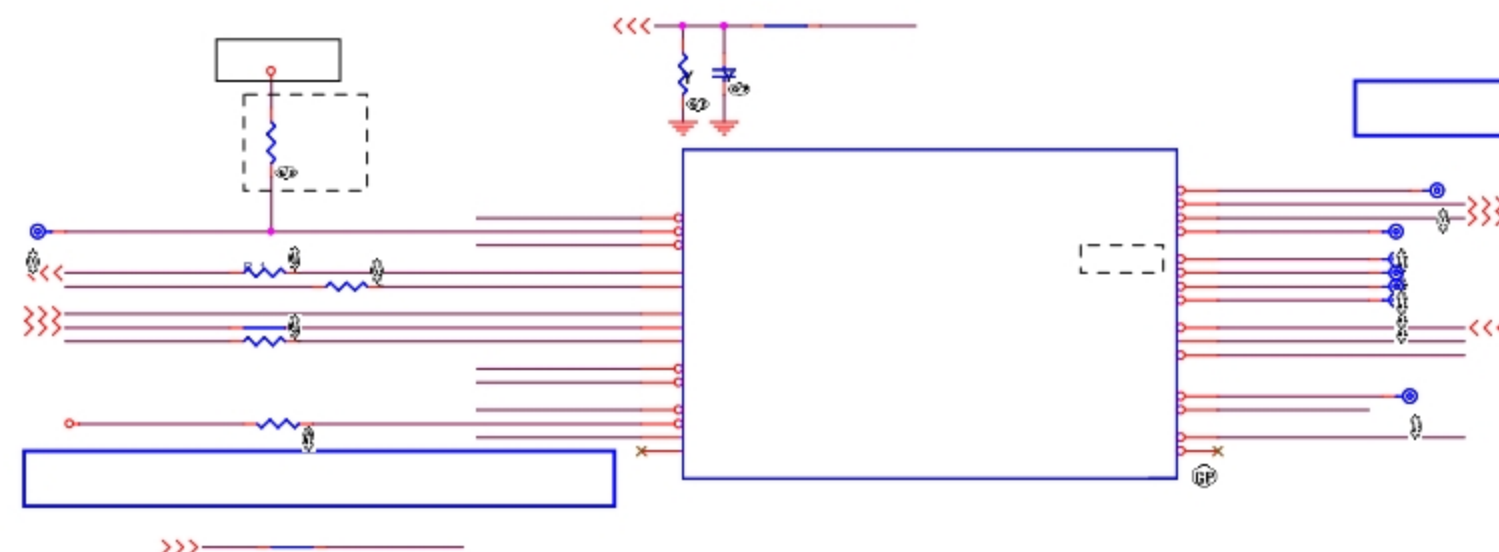
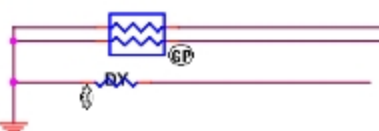
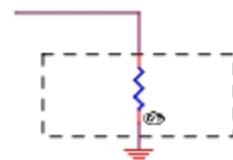
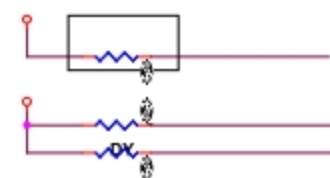
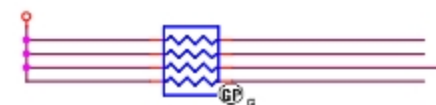
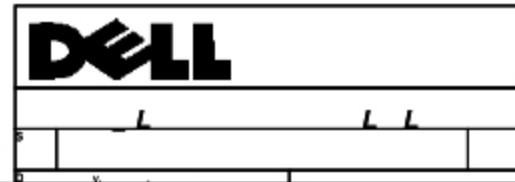
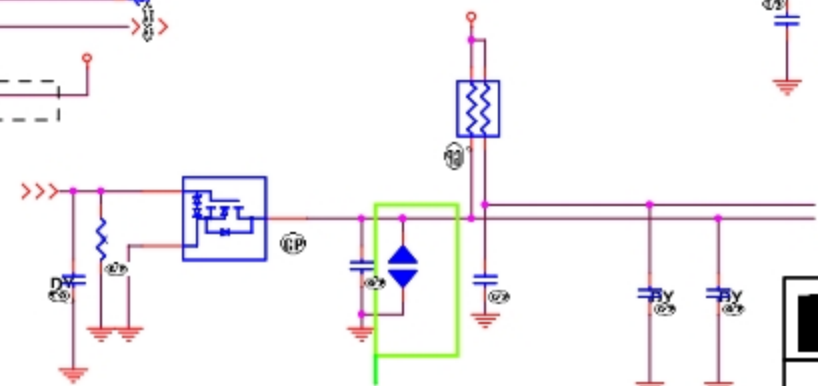
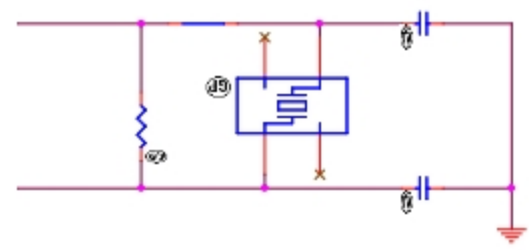
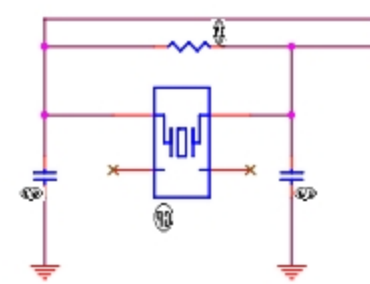
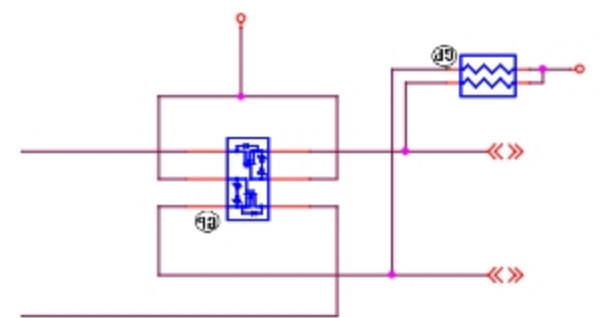
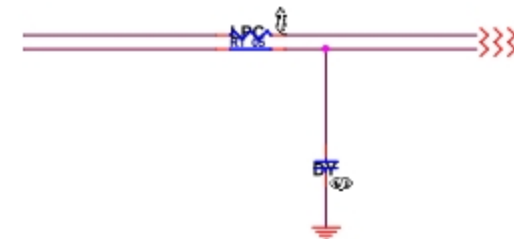
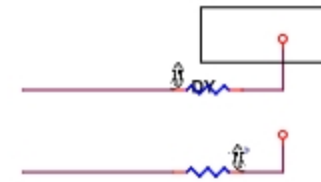
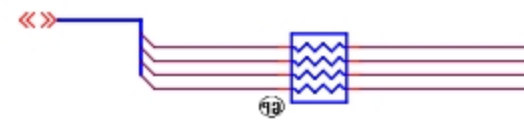
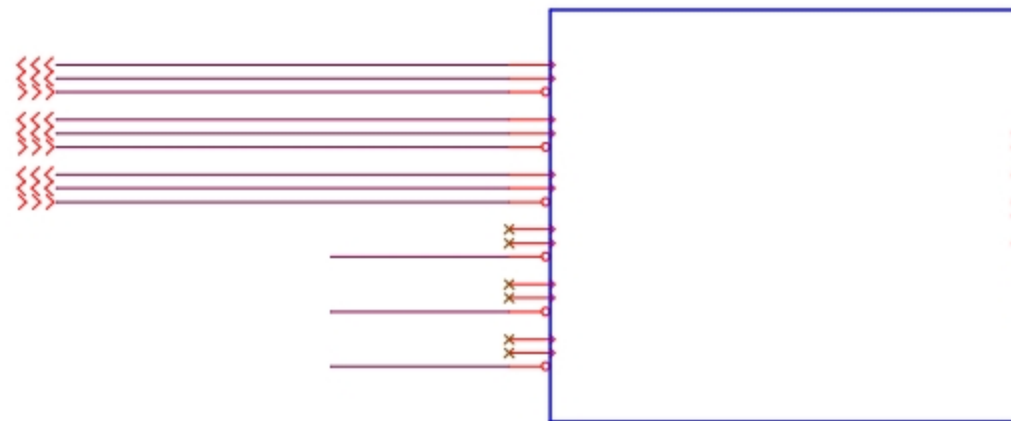
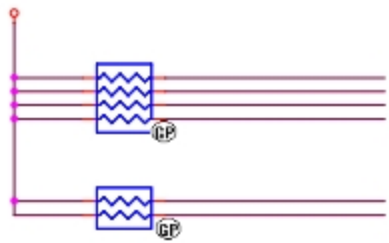
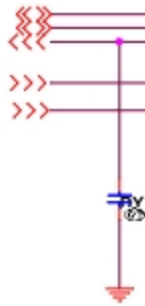
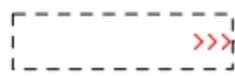
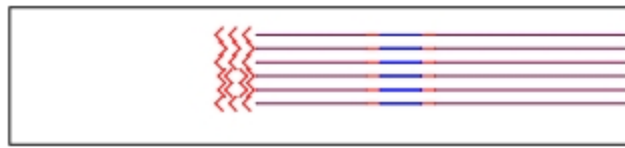
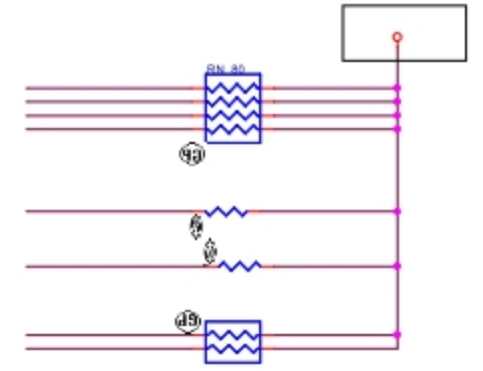
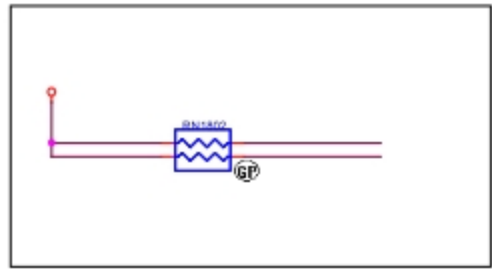


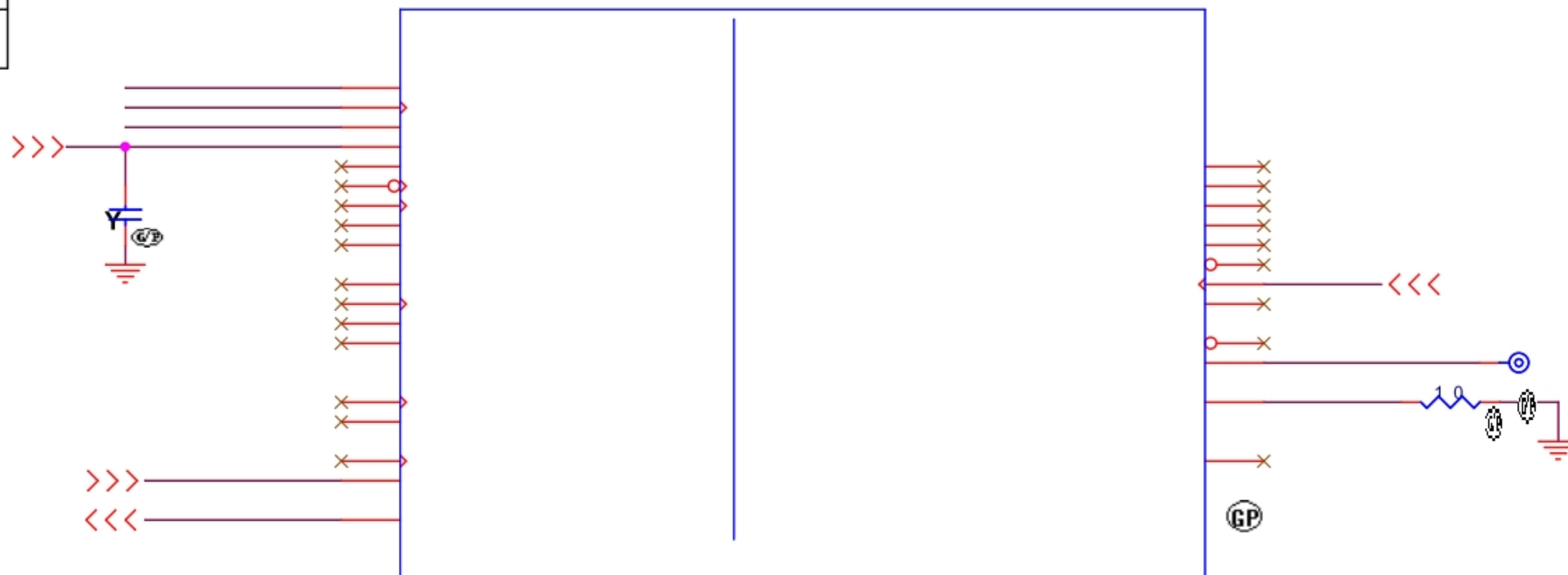
Table 24-3. PCI Express® Link Configurations Supported

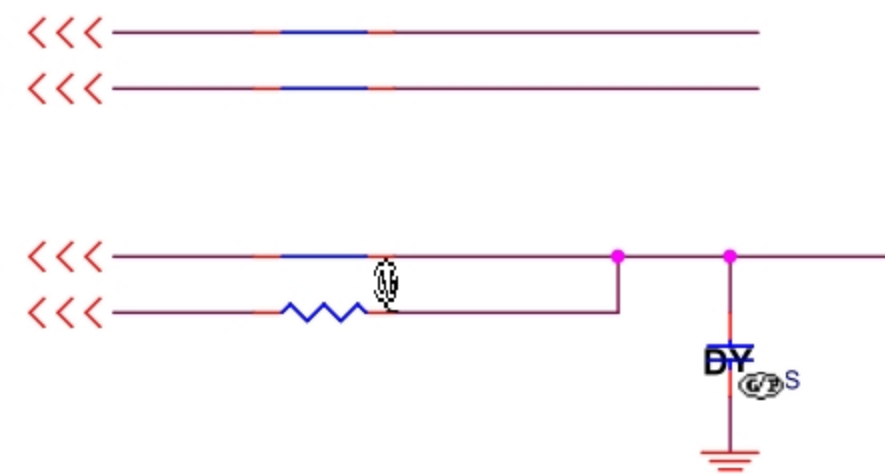
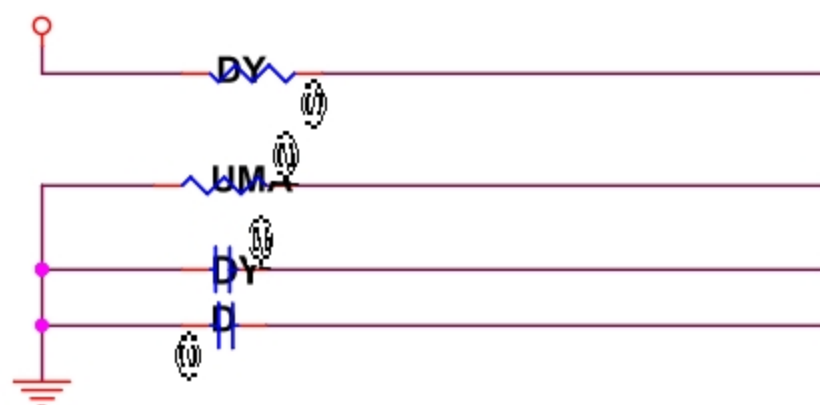
SKL	PCIe Link Config	PCI Express® Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3		Port5		Port7		Port9		Port11	
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3		Port5		Port7		Port9		Port11	
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
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	2x1	Port1		Port3		Port5		Port7		Port9		Port11	



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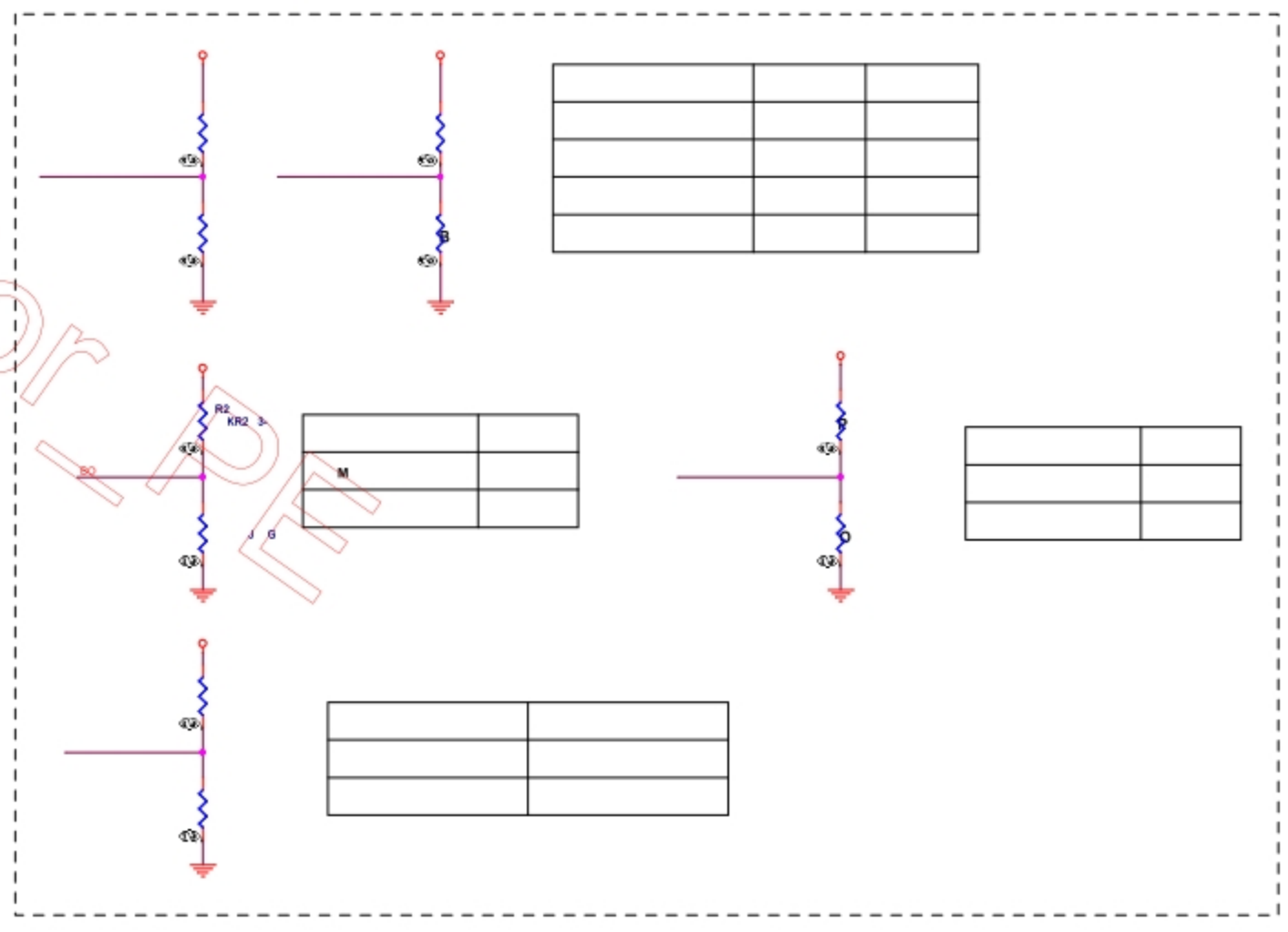
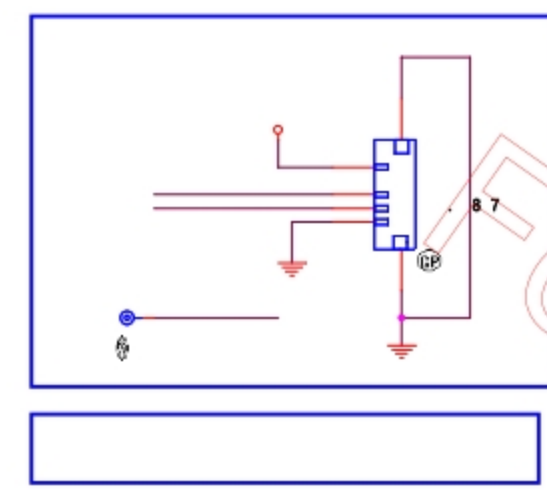
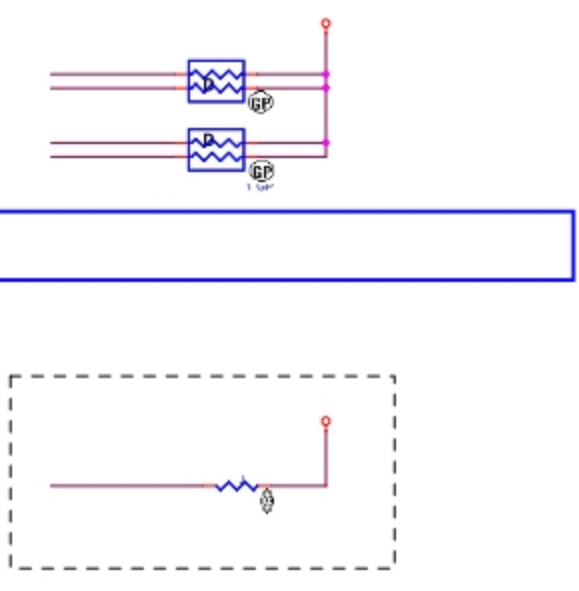
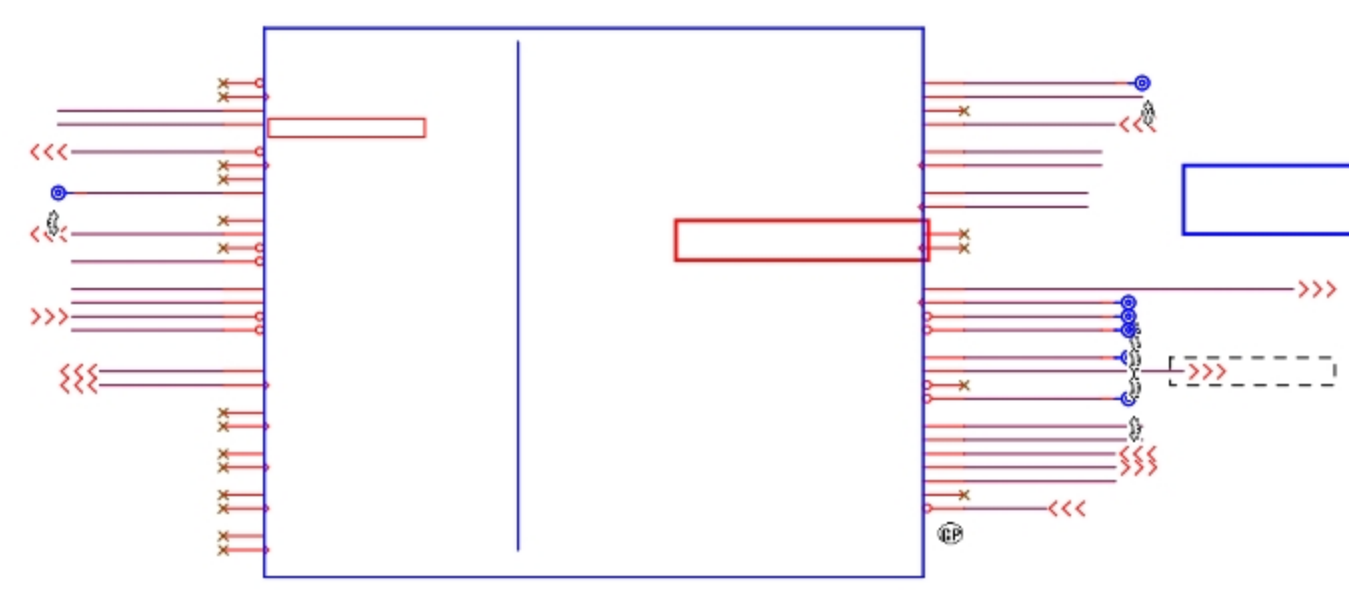
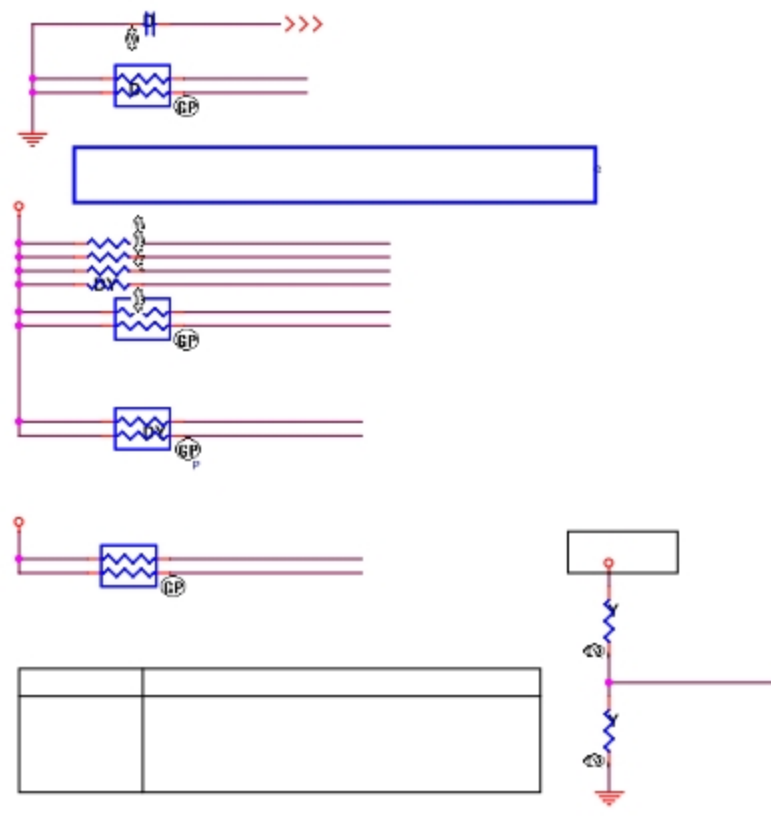


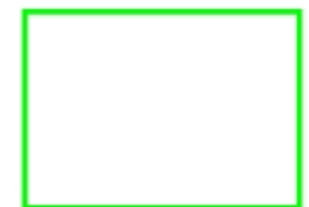
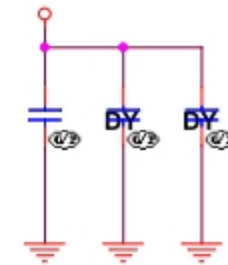
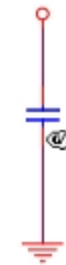
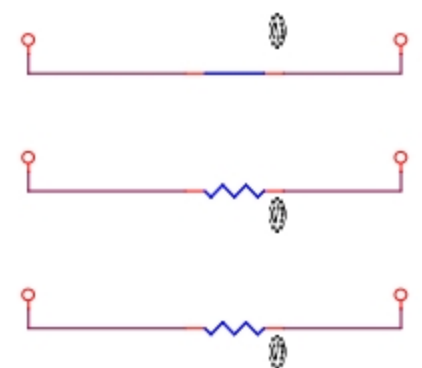
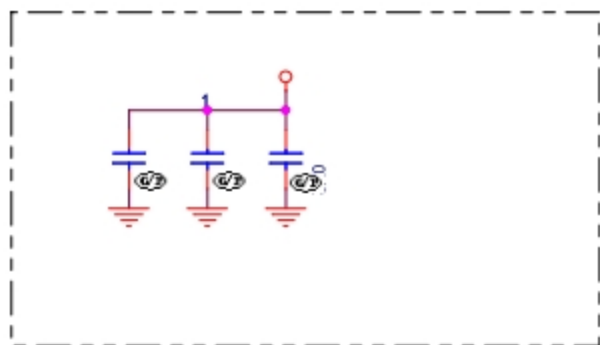
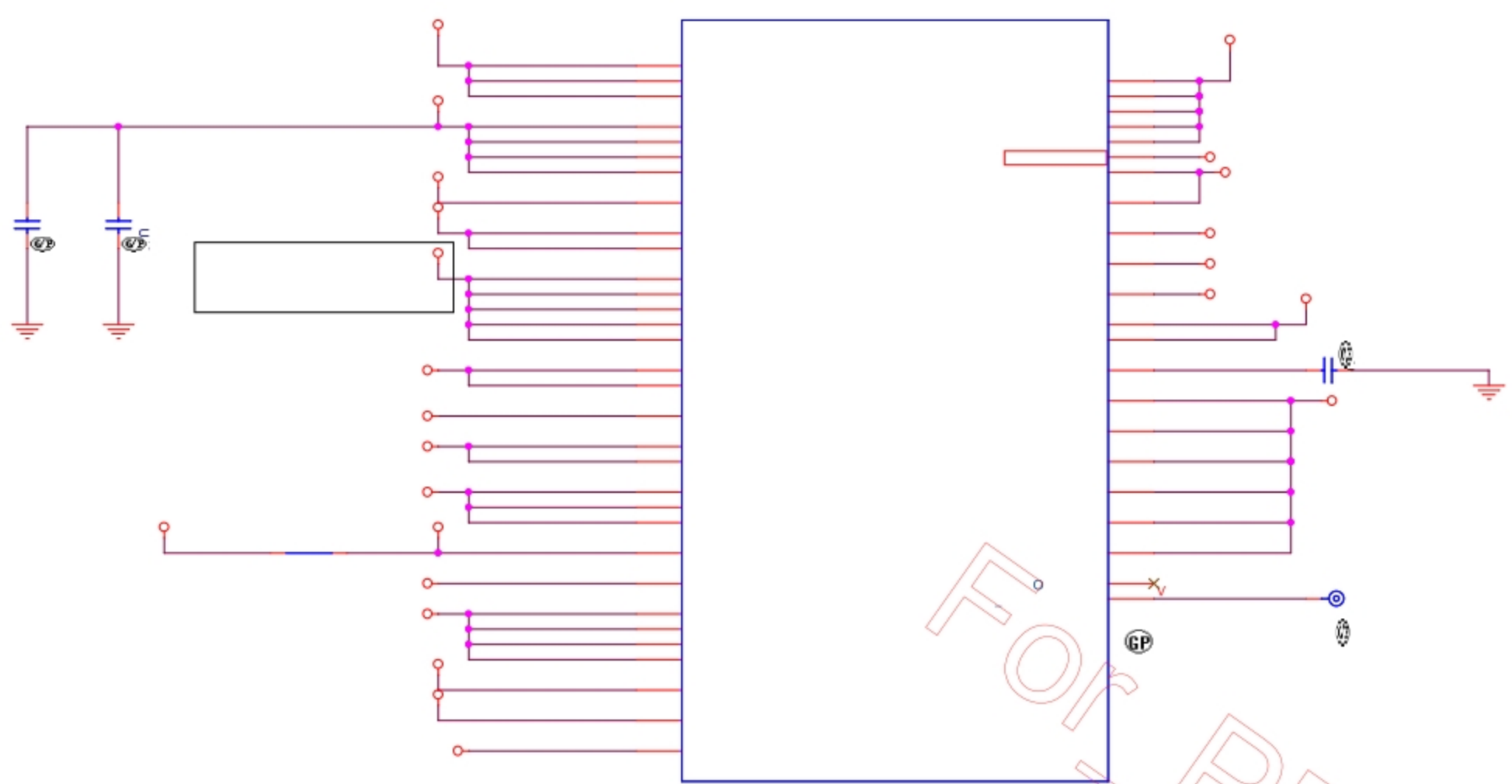



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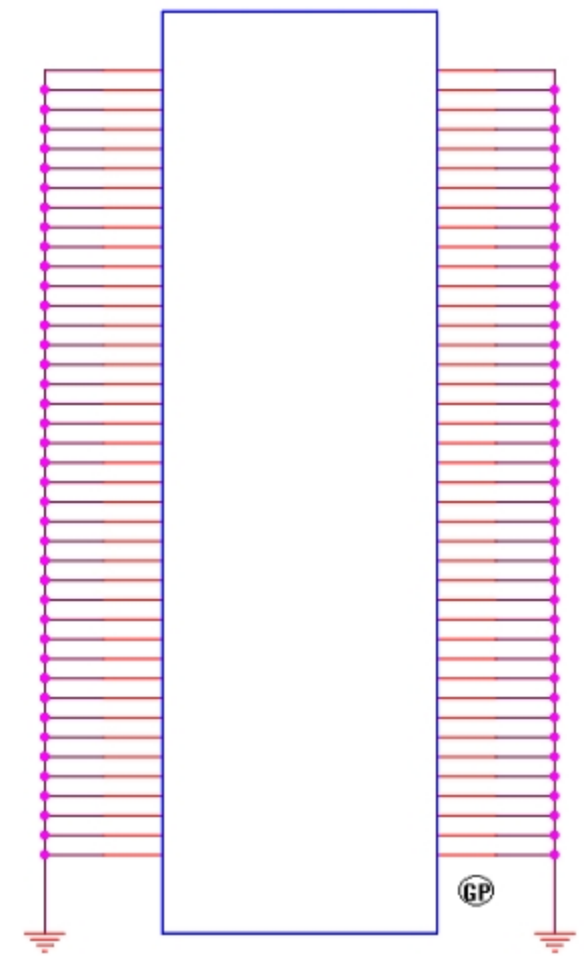
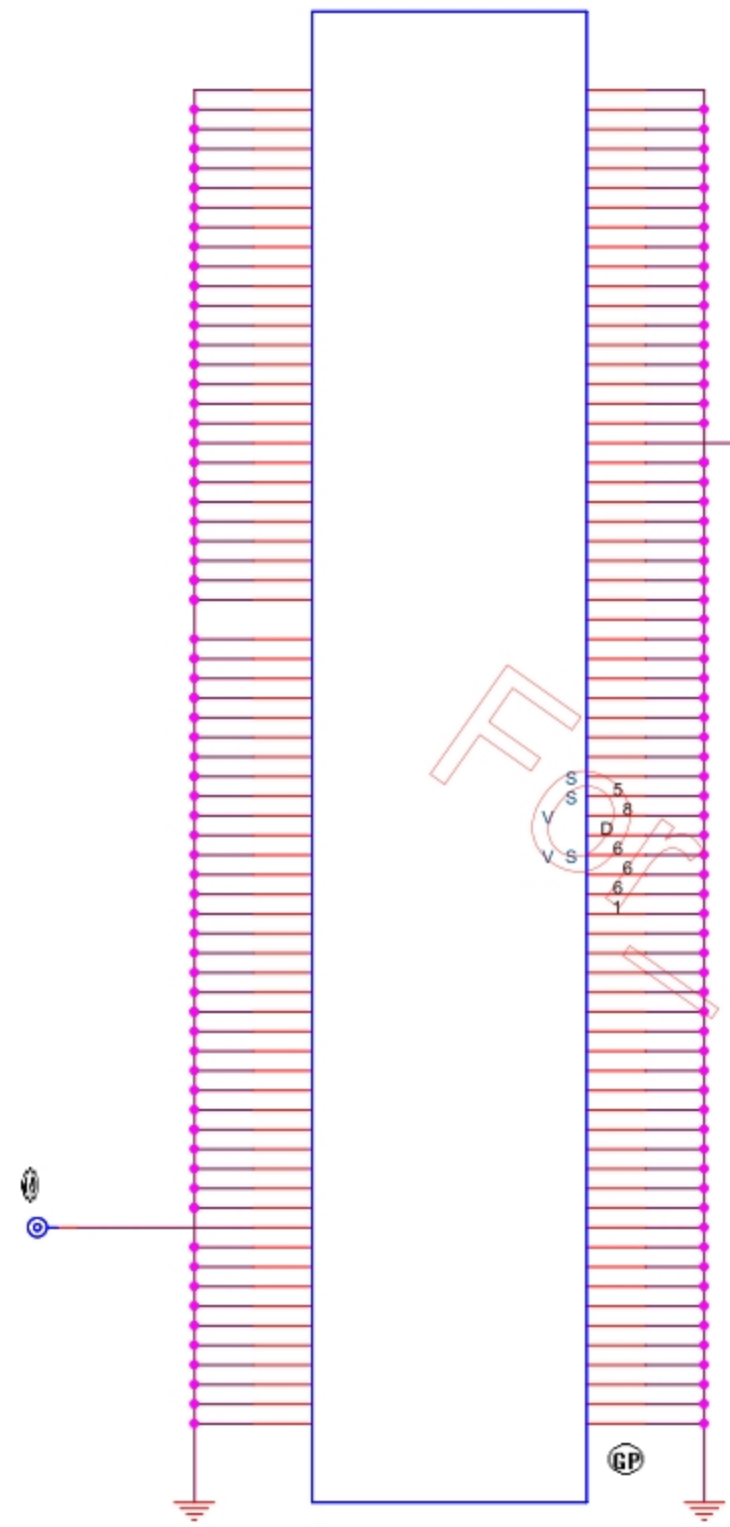
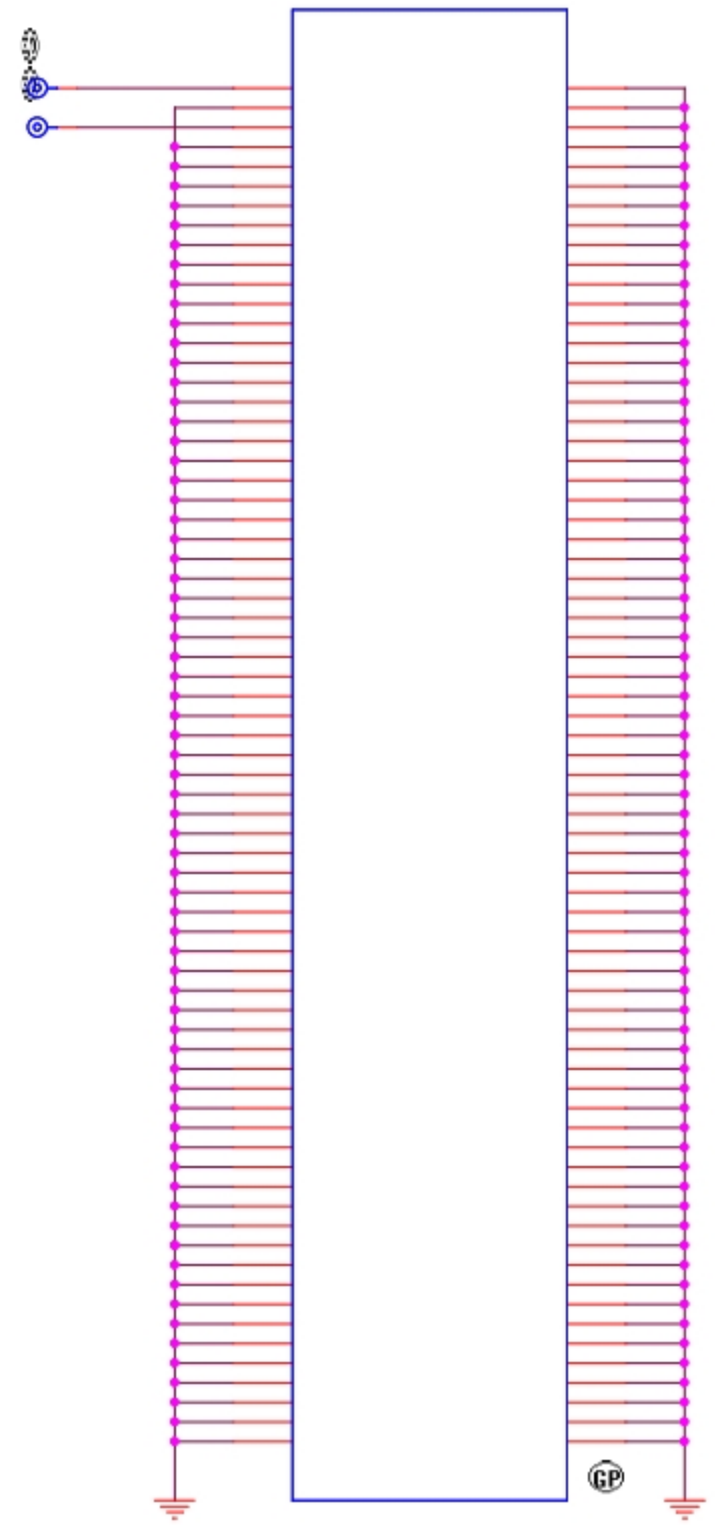




**DELL**

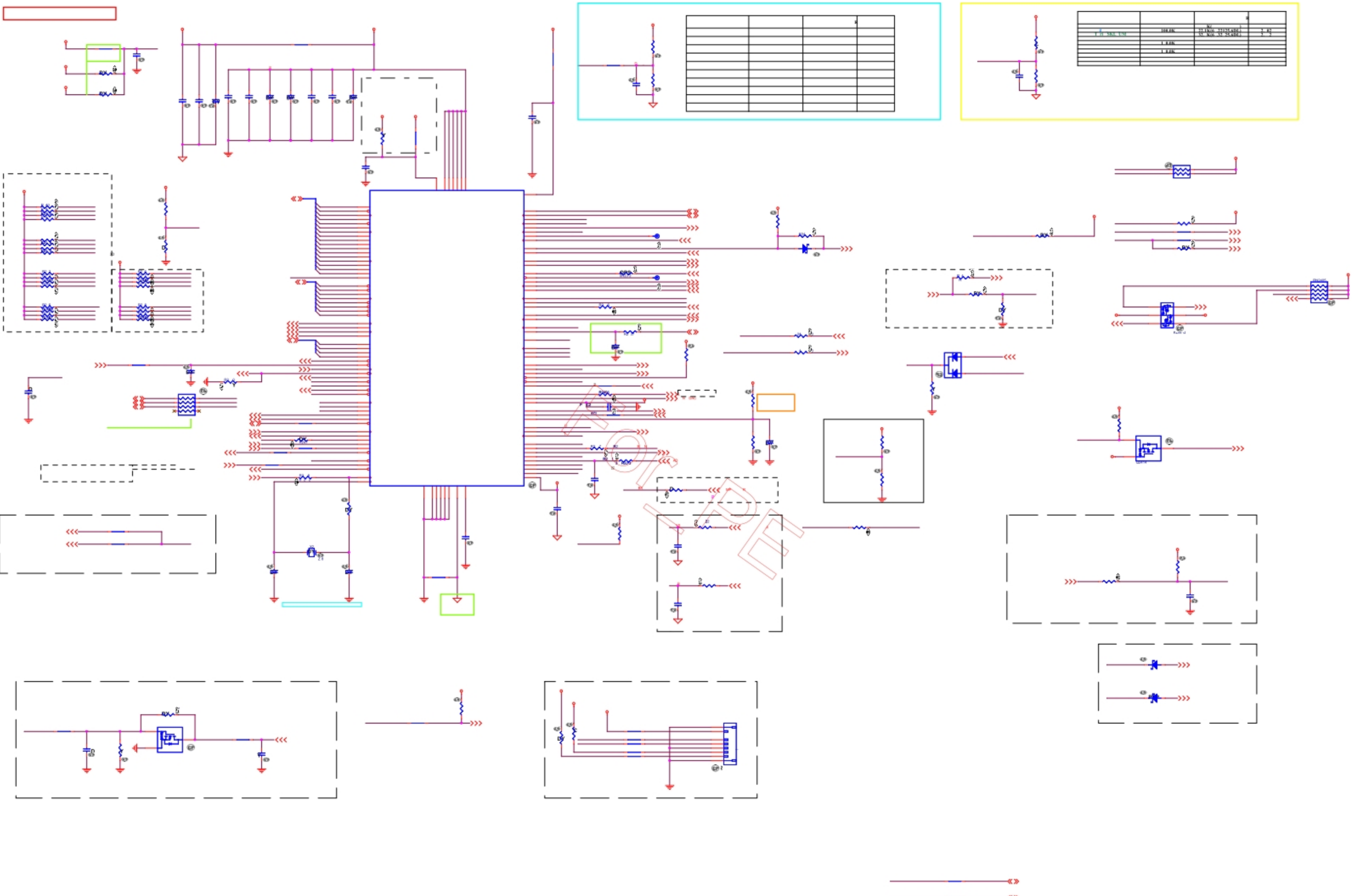
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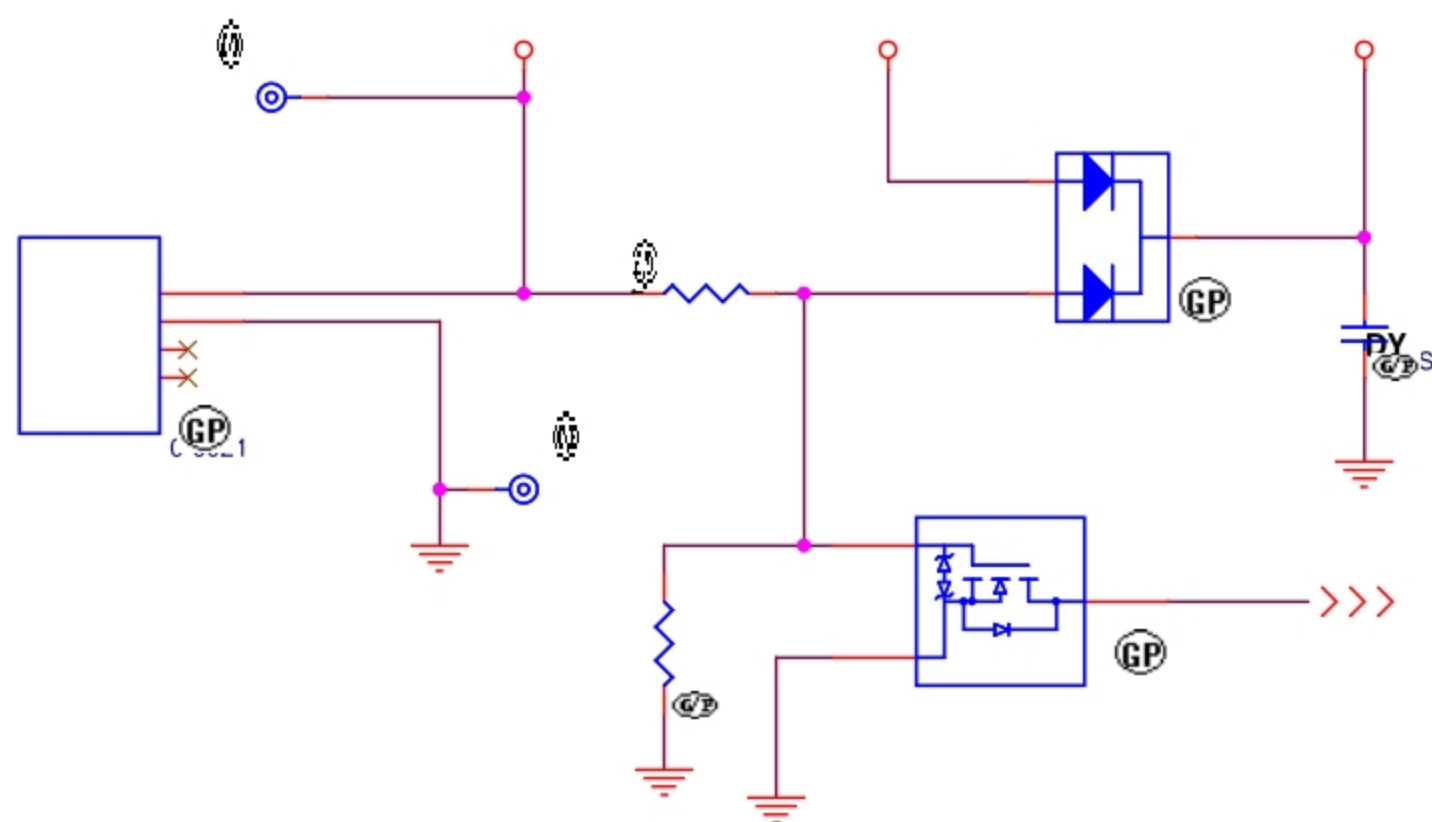
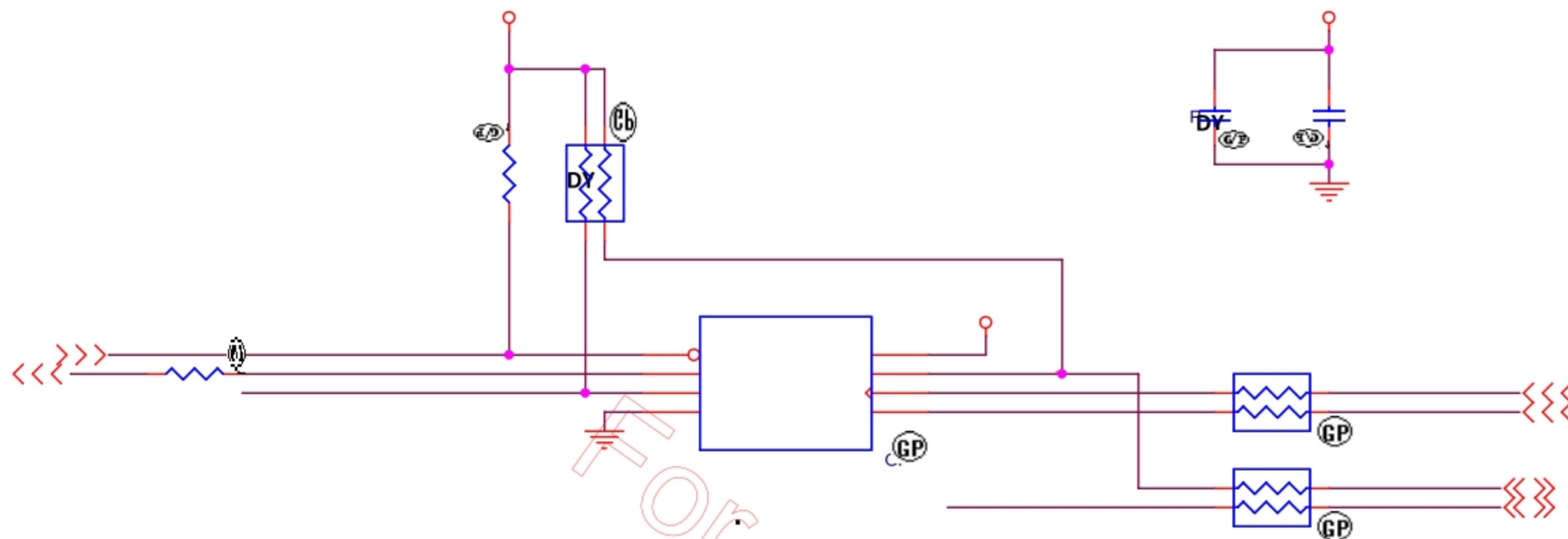
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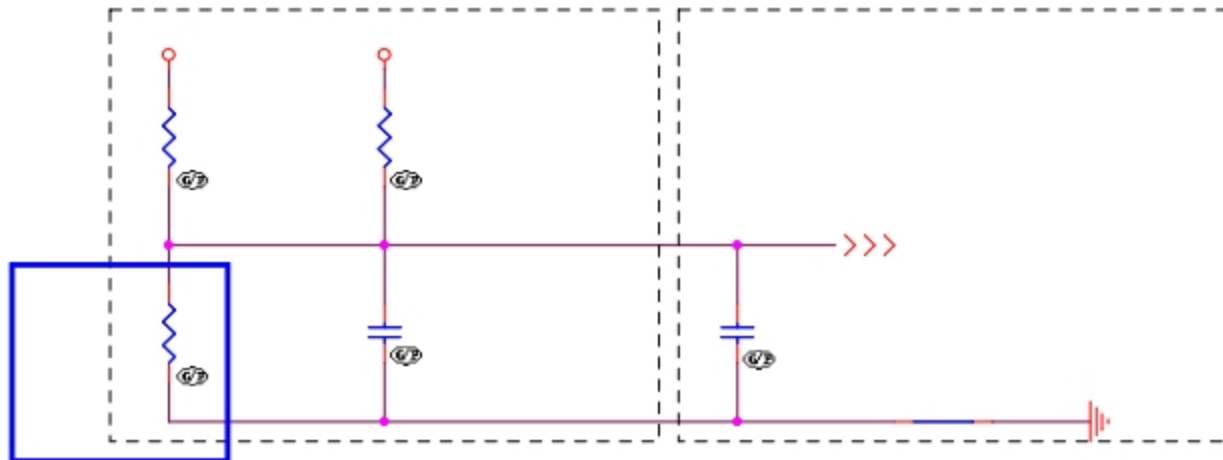
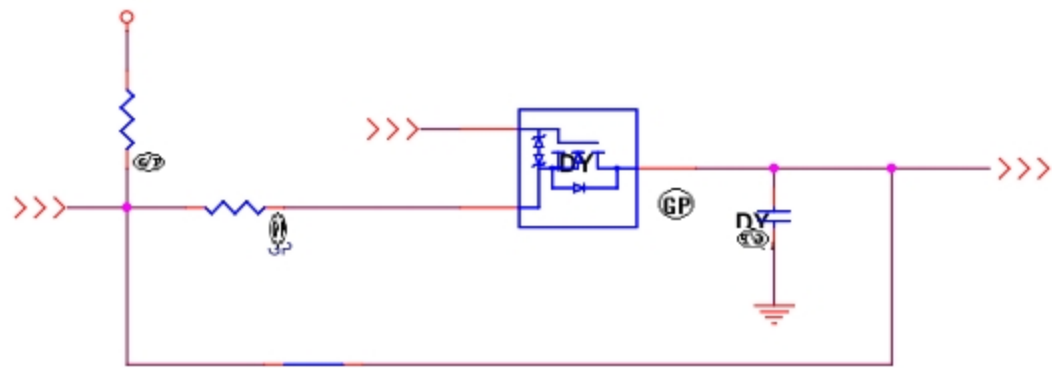
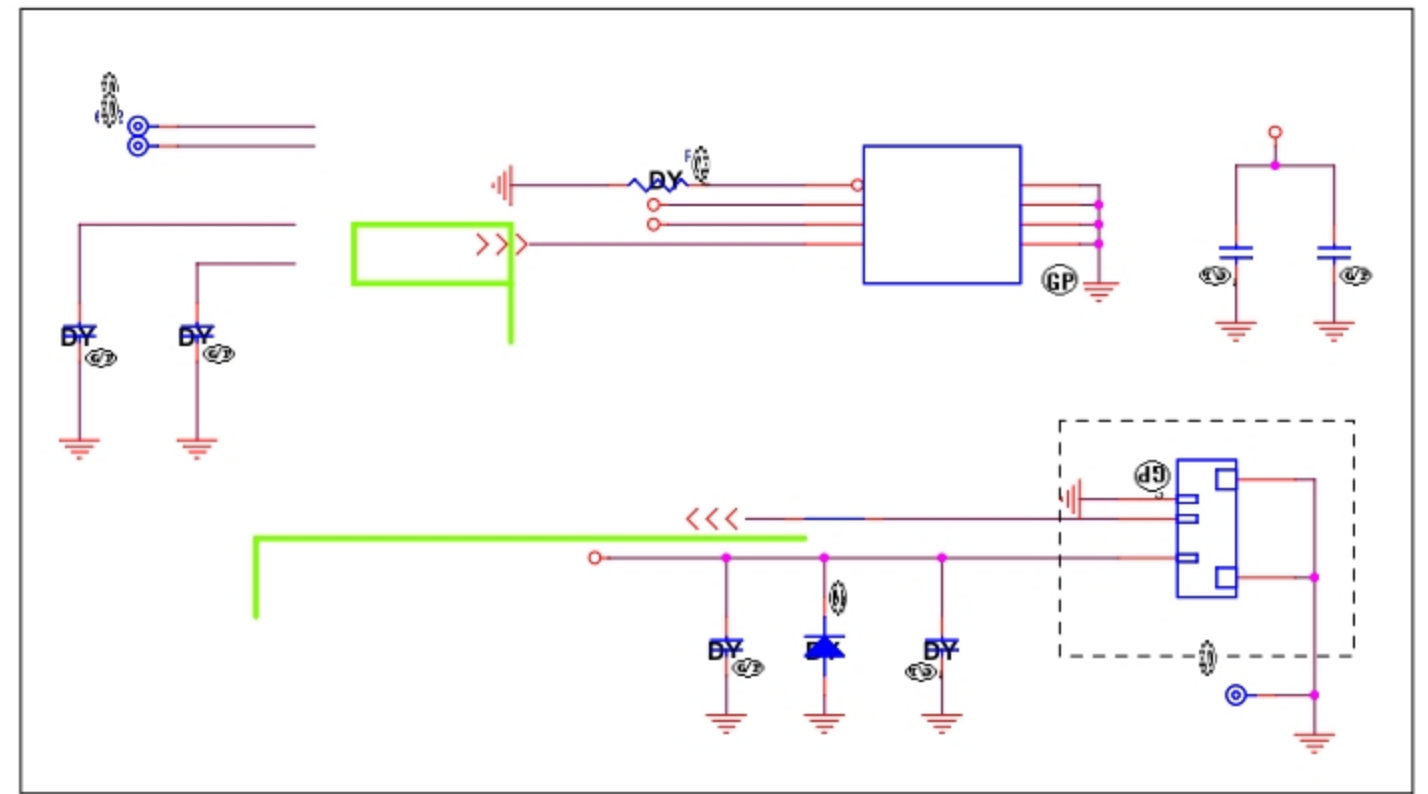
Skylake U Processor Corner NCTF Motherboard Test Point Example

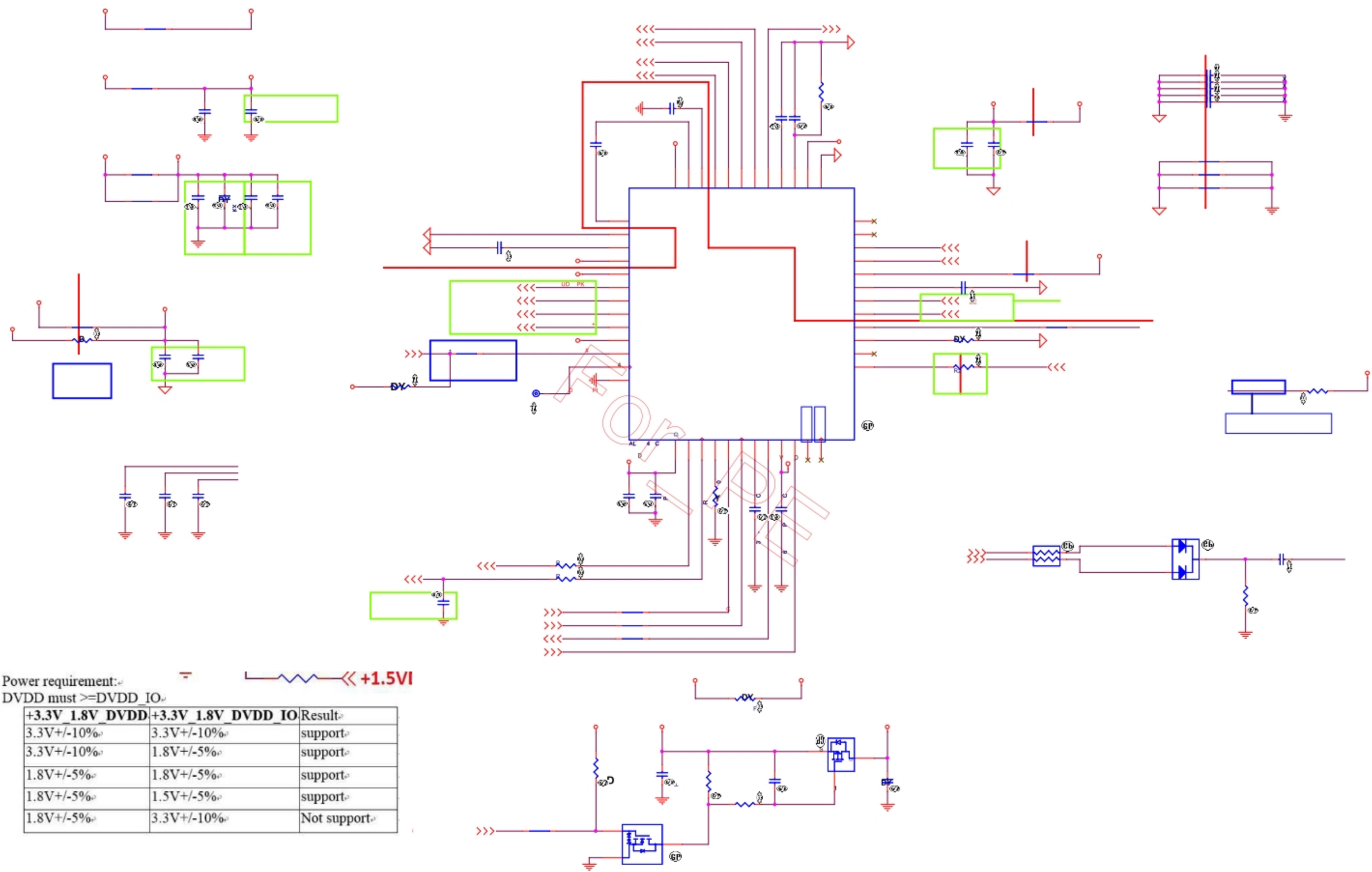
Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	Corner A71
A70	NCTFVSS	Test Point (TP)	
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	





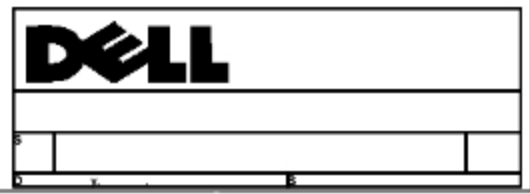
**DELL**





Power requirement:  
 DVDD must >=DVDD\_IO

+3.3V	1.8V	DVDD	+3.3V	1.8V	DVDD	IO	Result
3.3V+/-10%			3.3V+/-10%				support
3.3V+/-10%			1.8V+/-5%				support
1.8V+/-5%			1.8V+/-5%				support
1.8V+/-5%			1.5V+/-5%				support
1.8V+/-5%			3.3V+/-10%				Not support



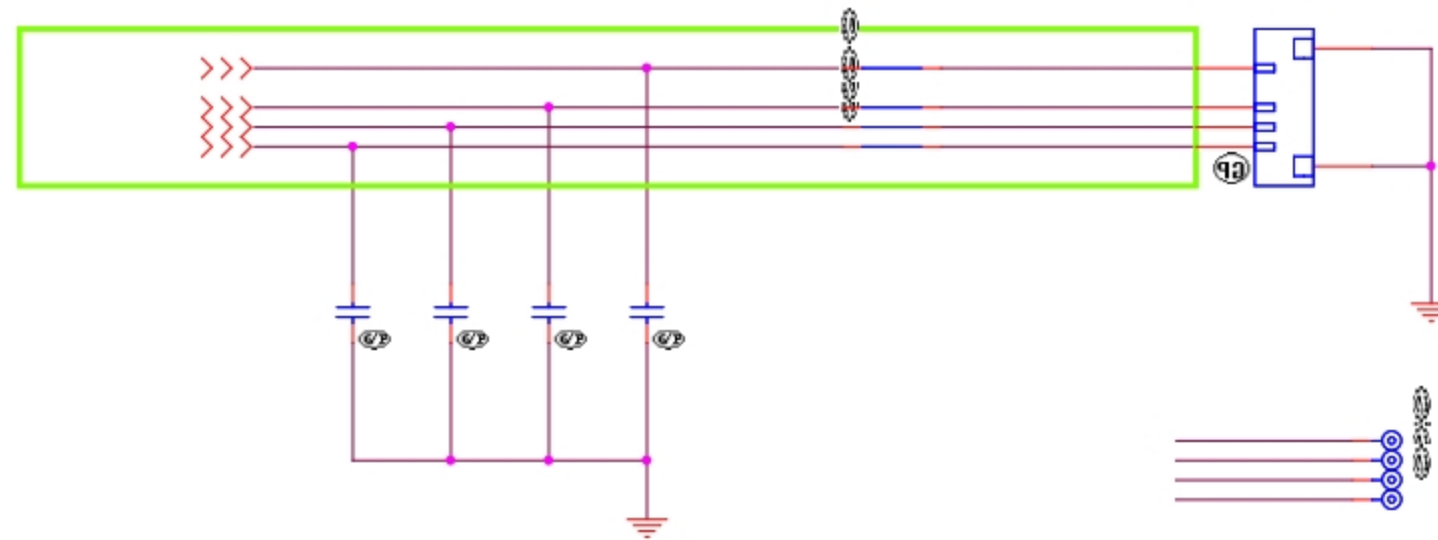
For PE

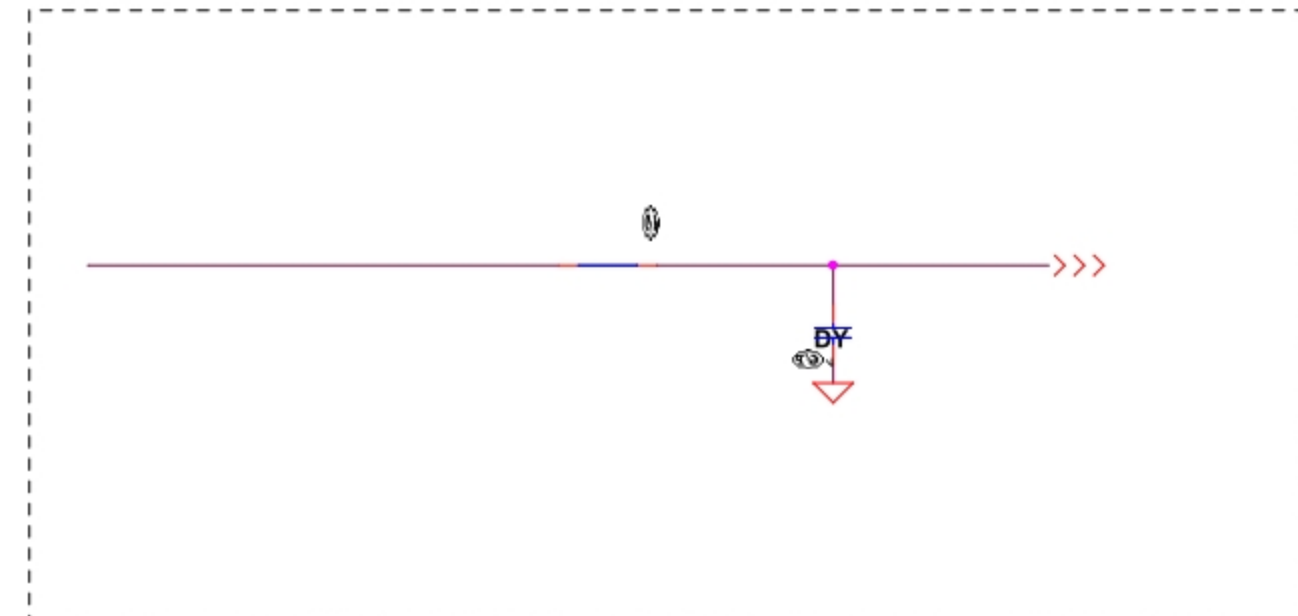
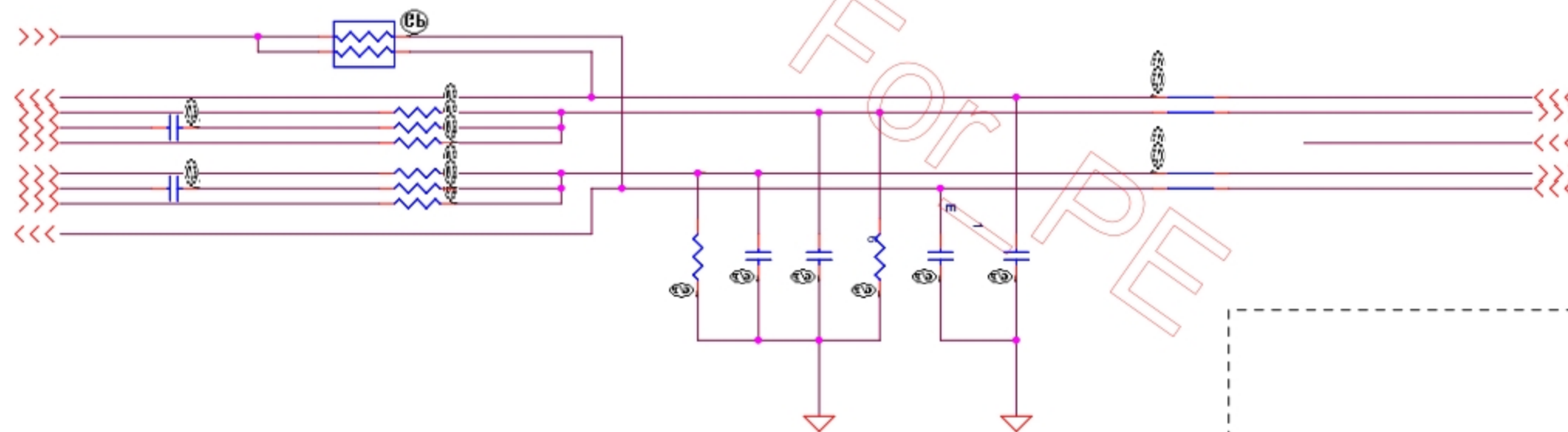
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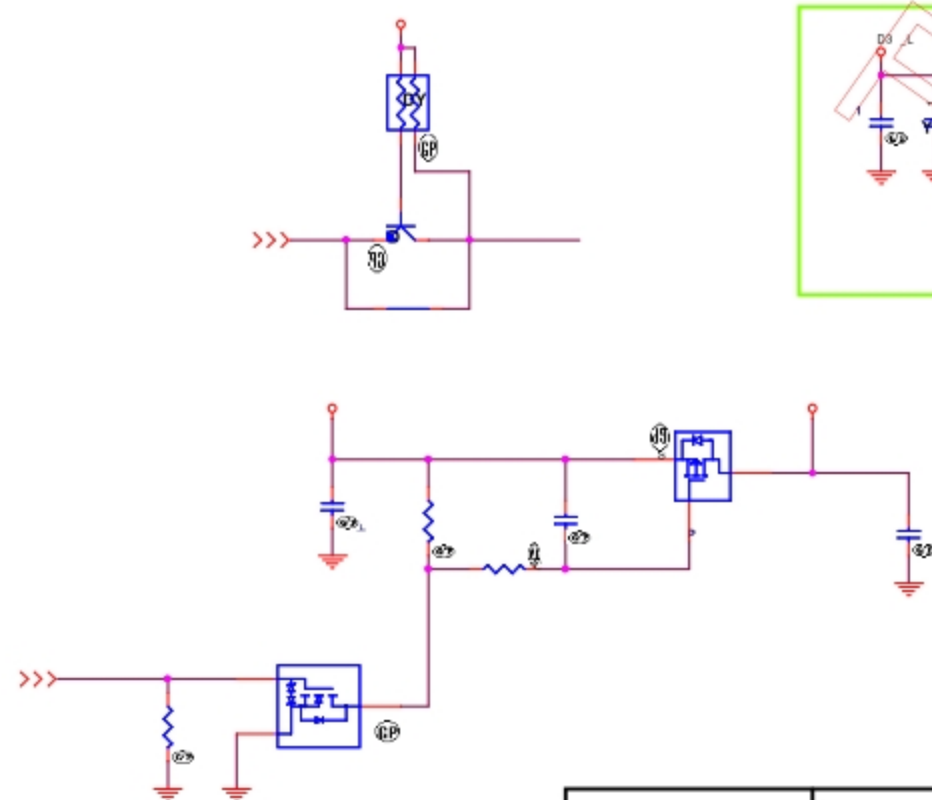
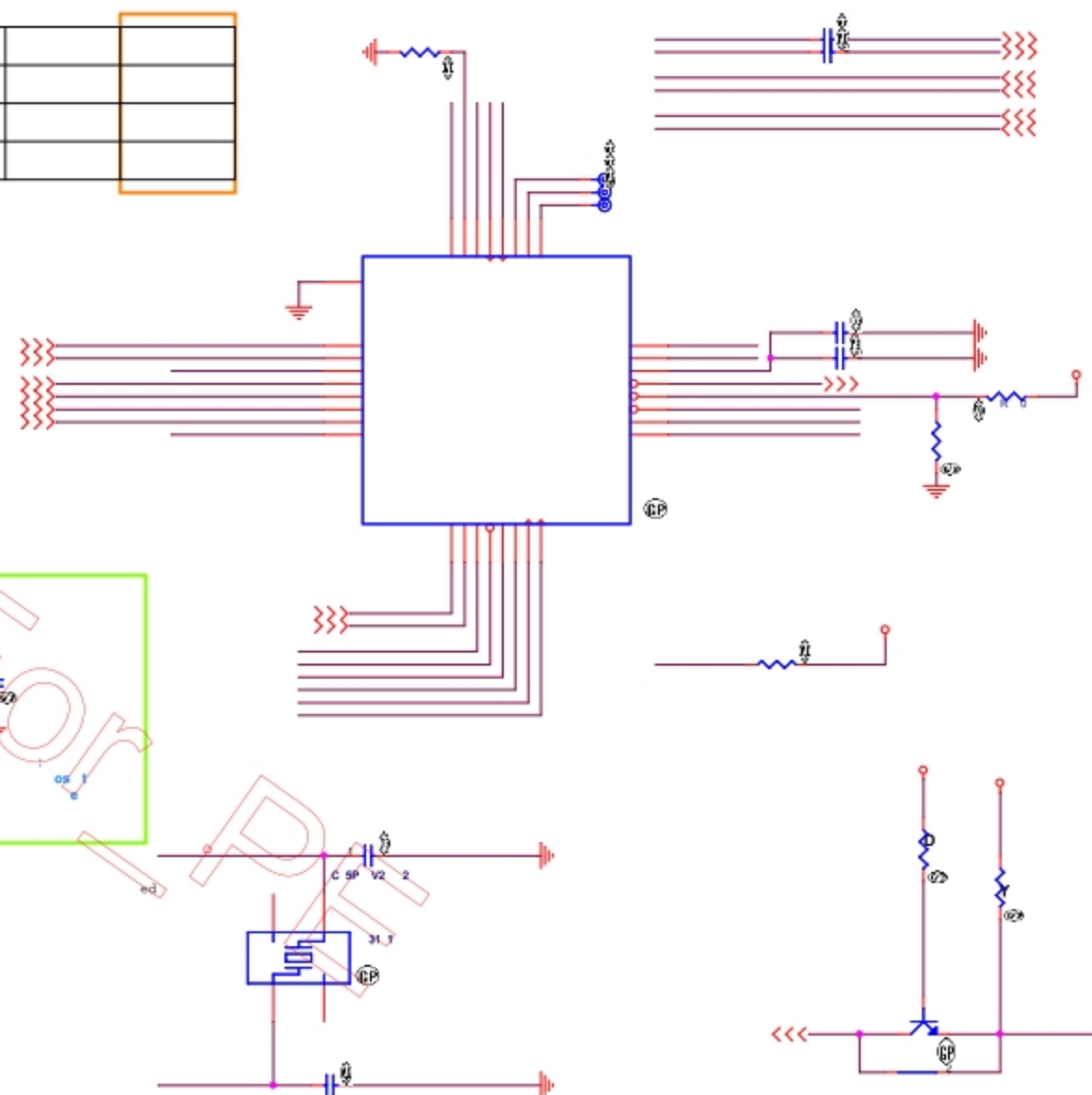
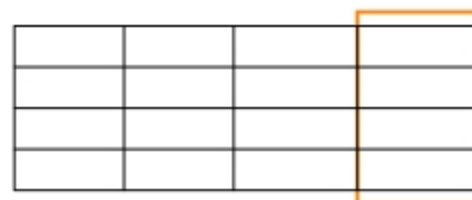


For PE

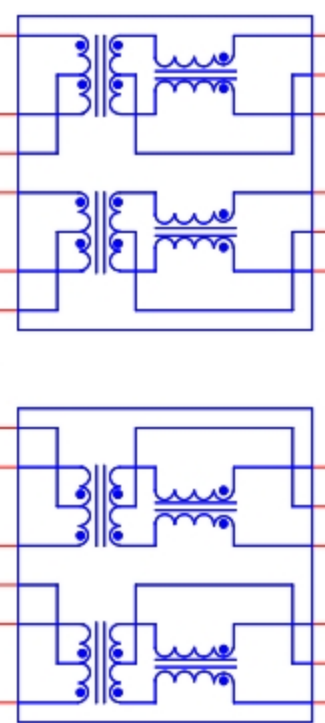
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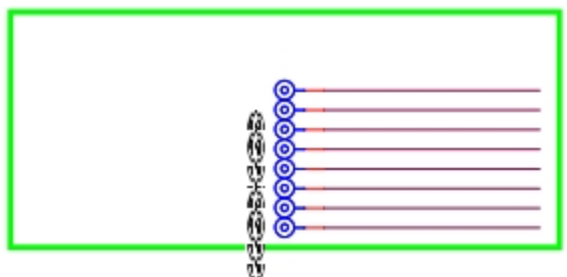
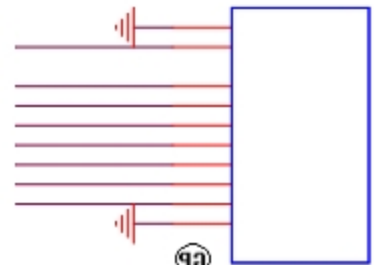
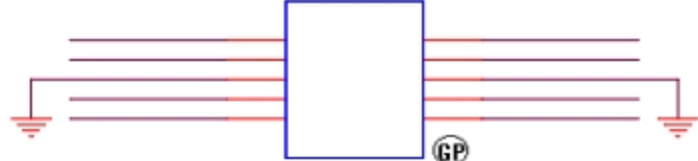
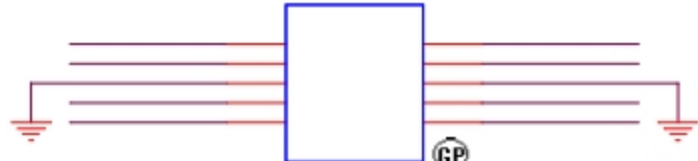
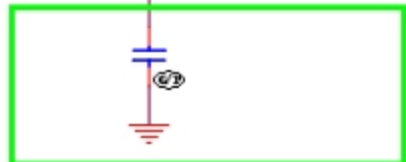
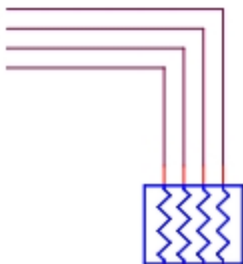
[illegible]



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FOR PE

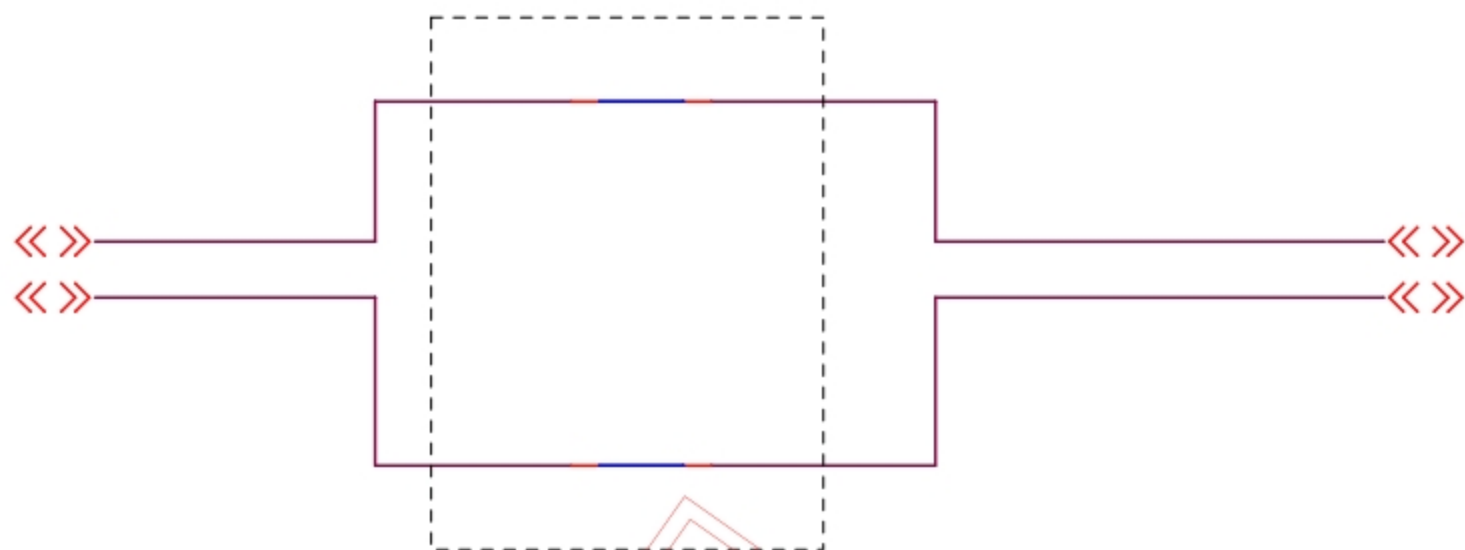


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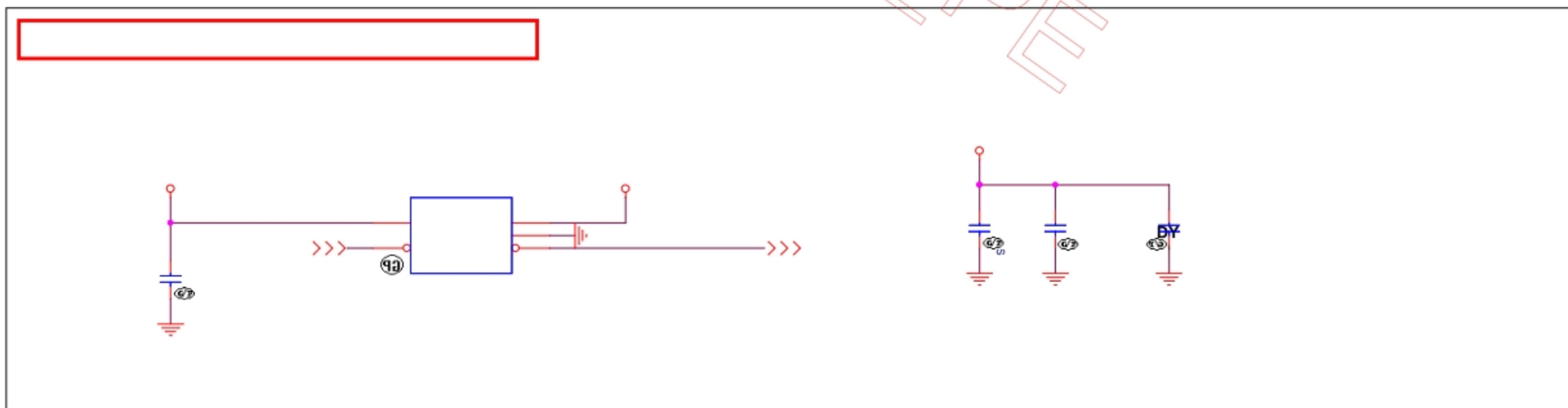
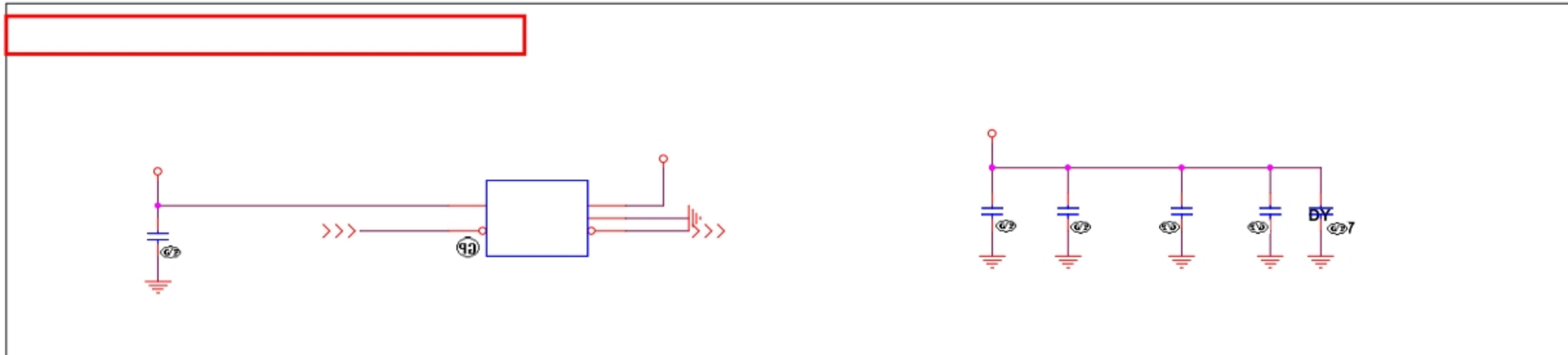
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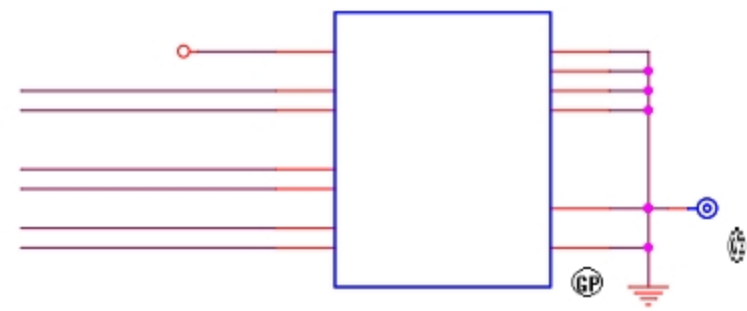
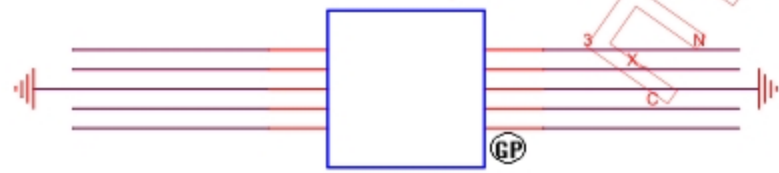
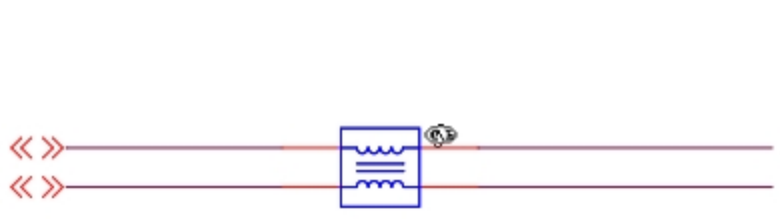
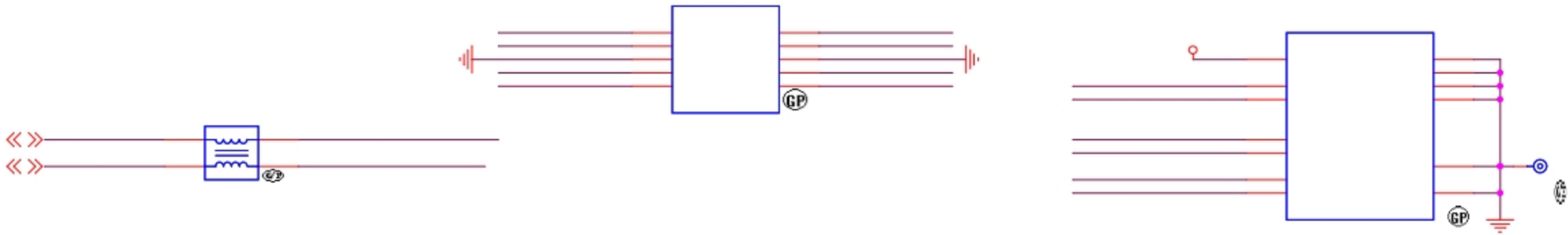
For PE

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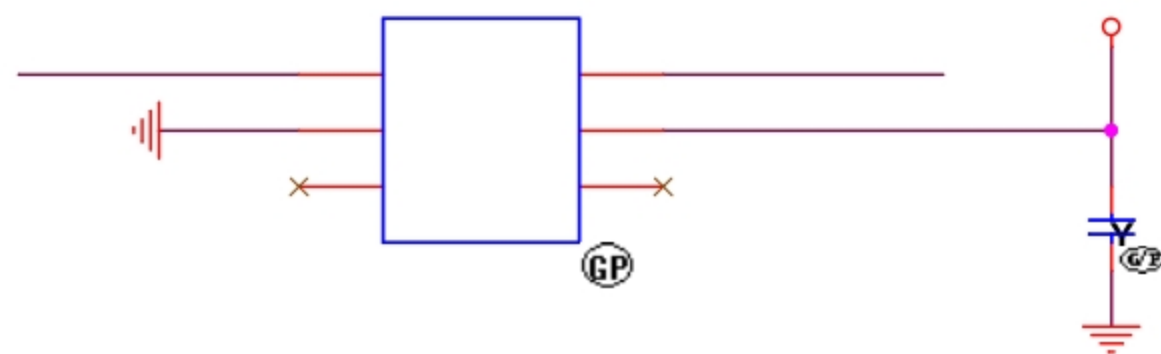
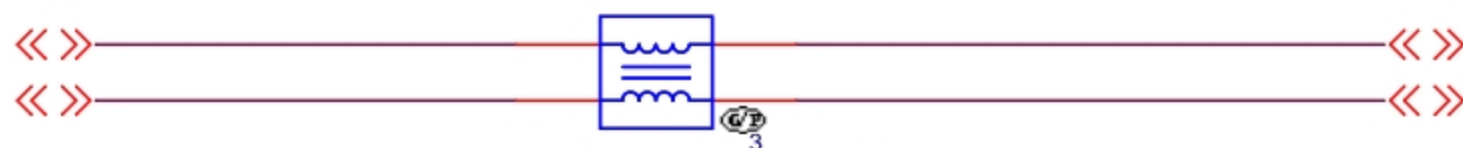
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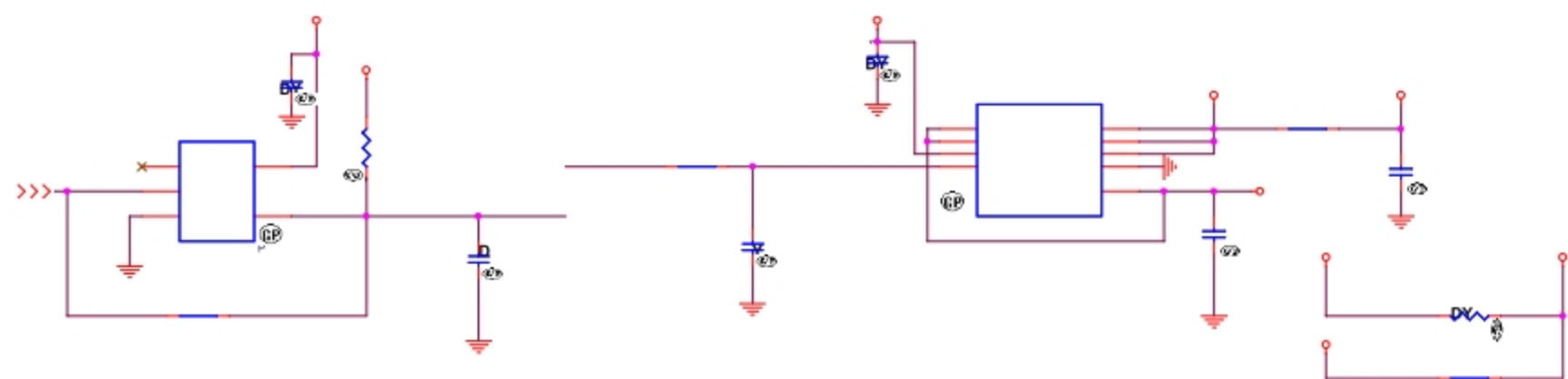
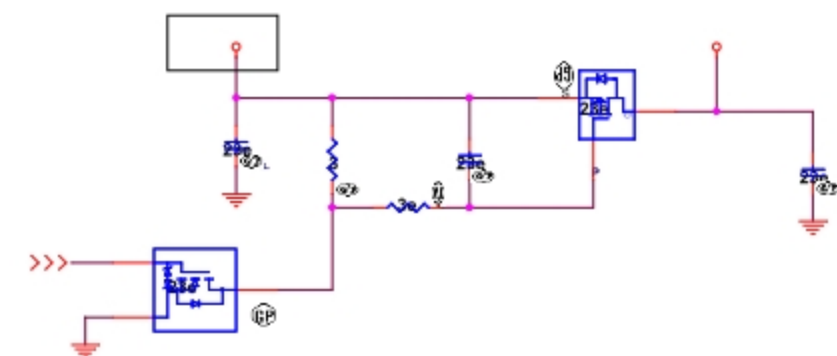
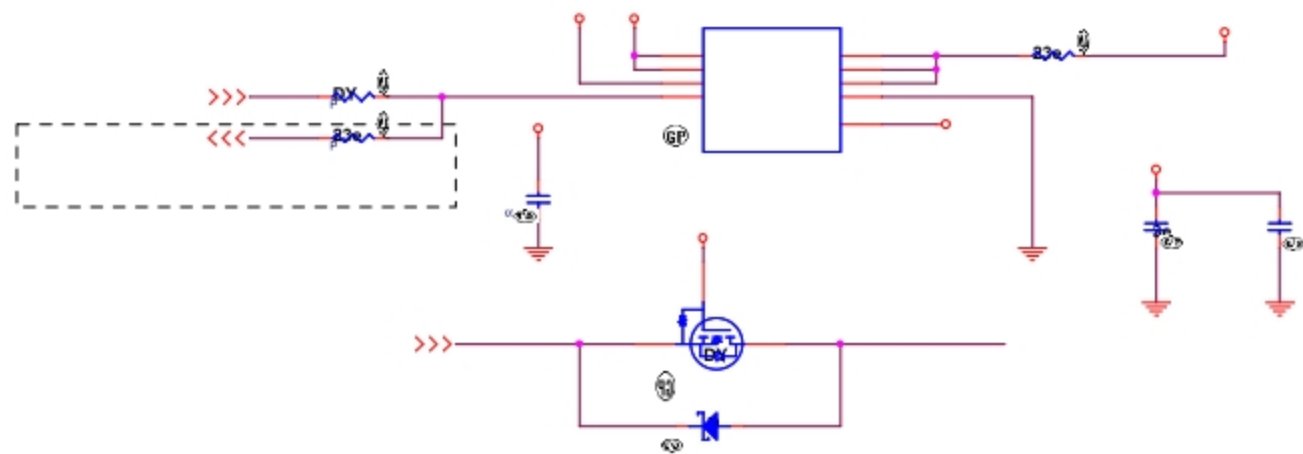
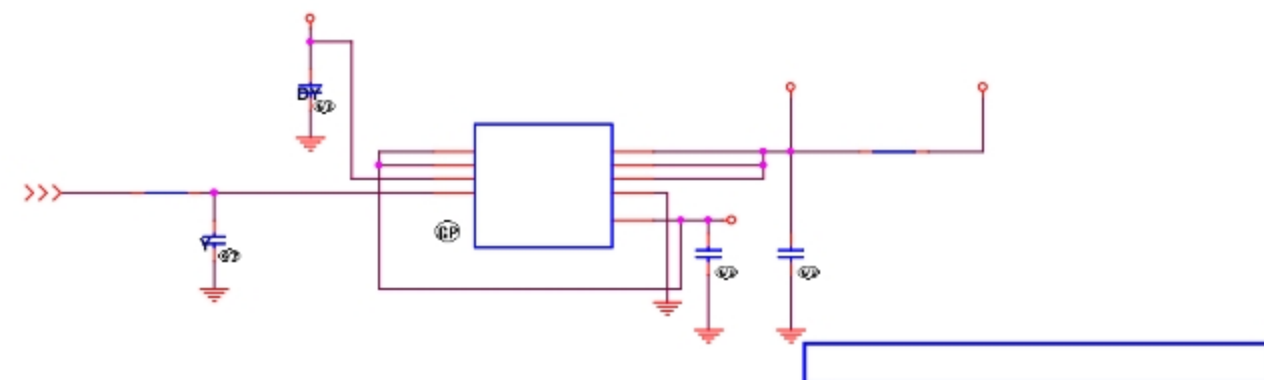
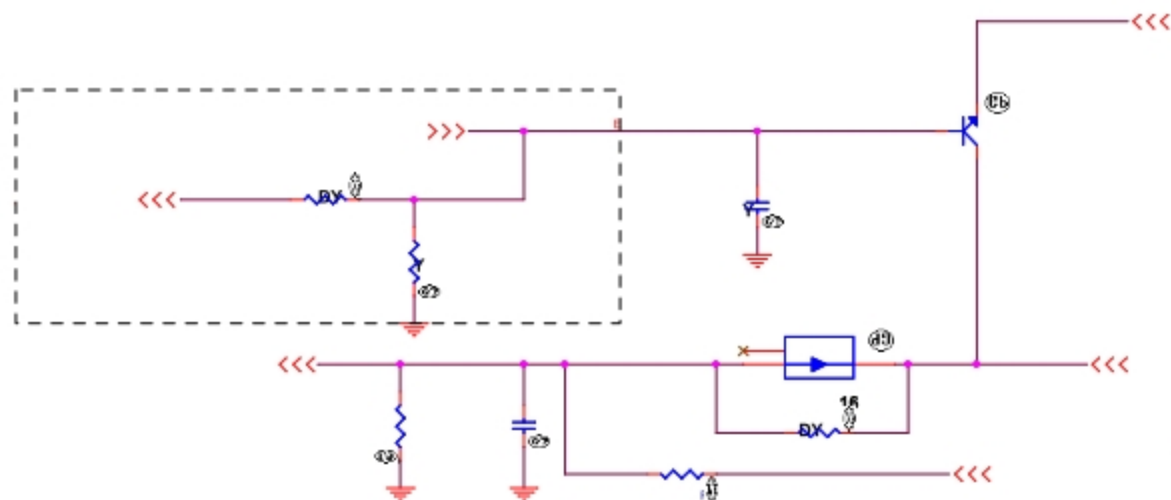
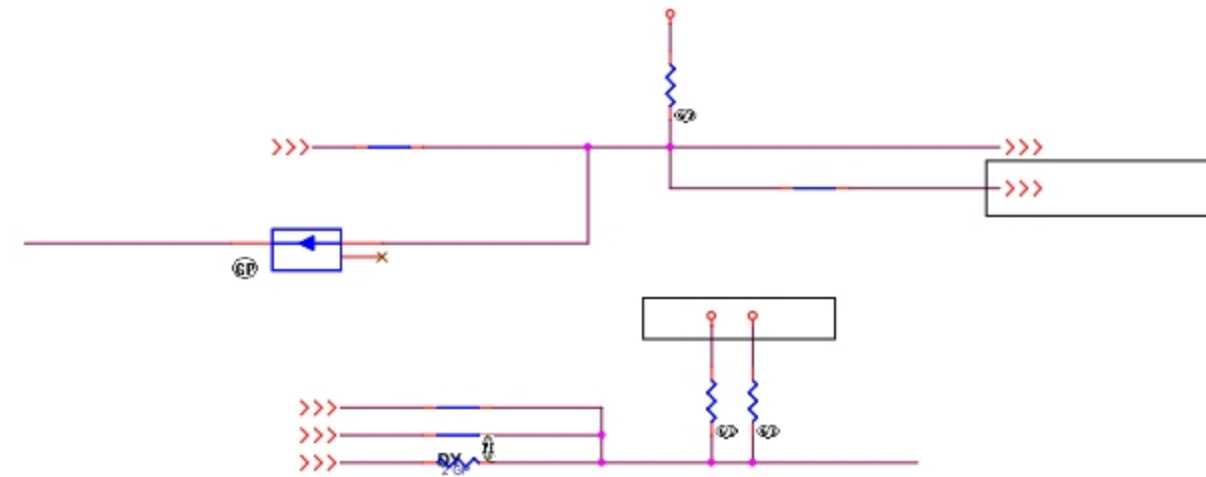
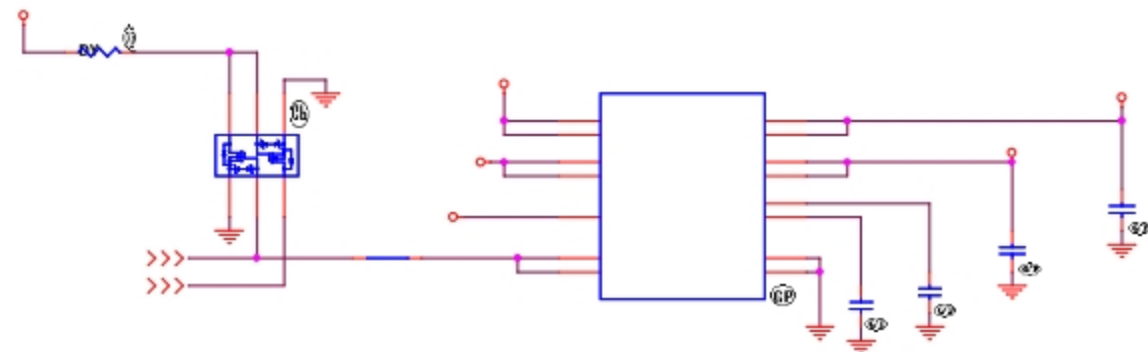
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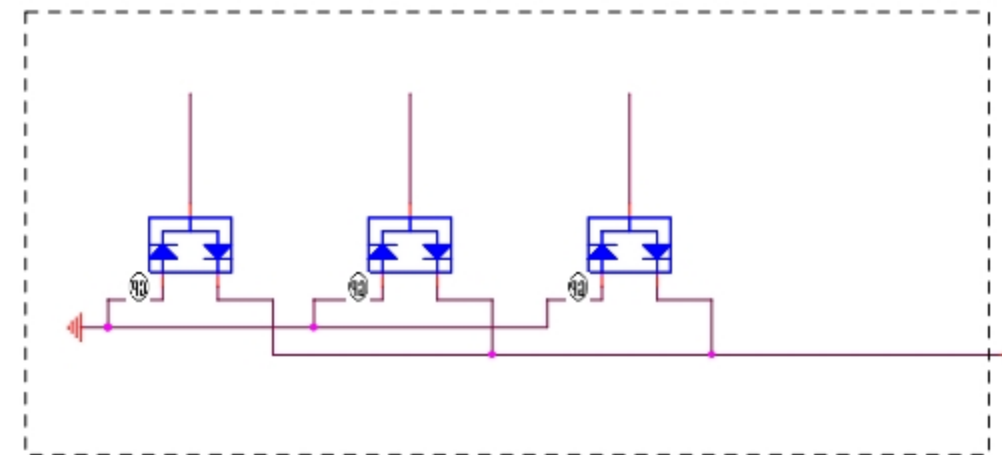
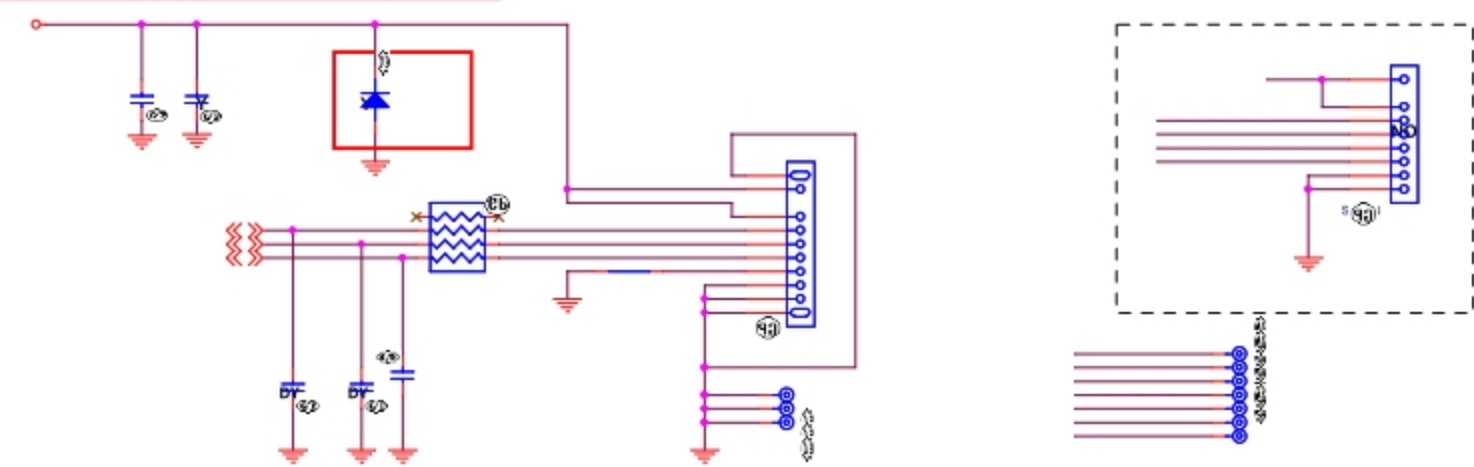
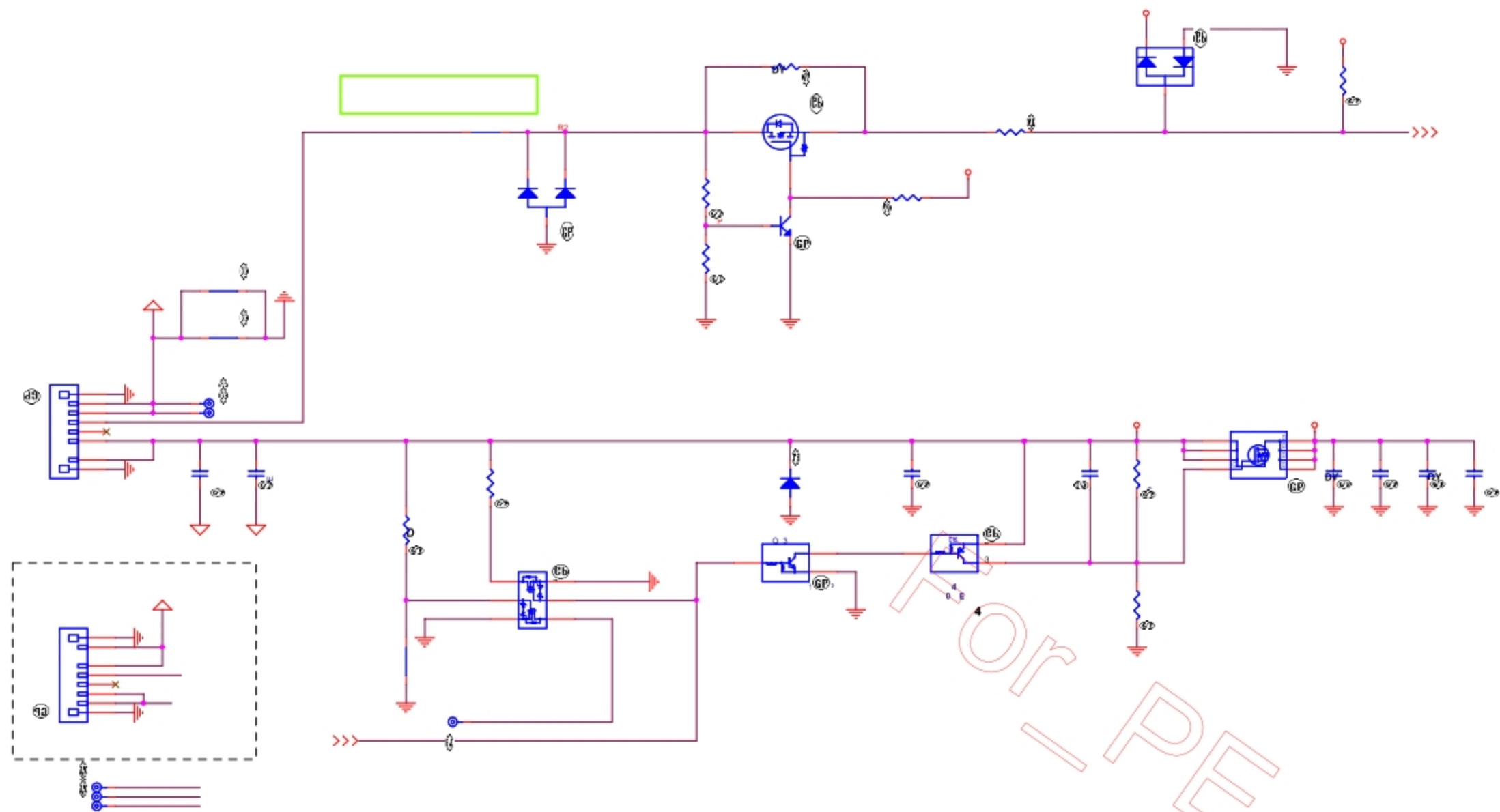


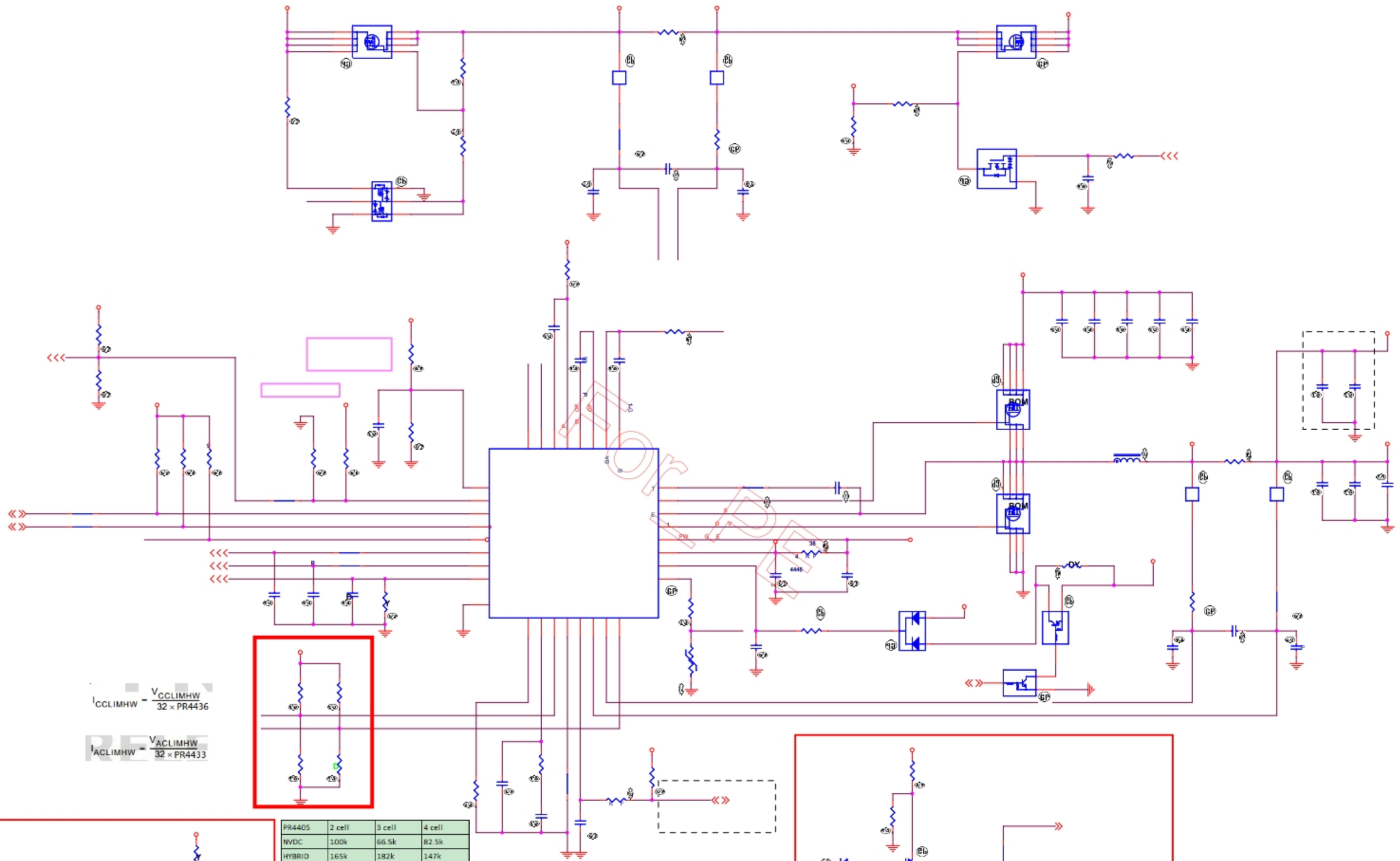
For PE

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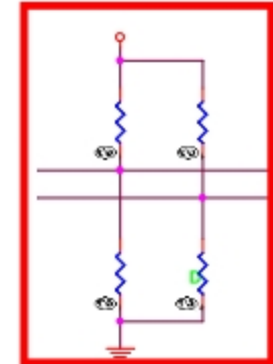
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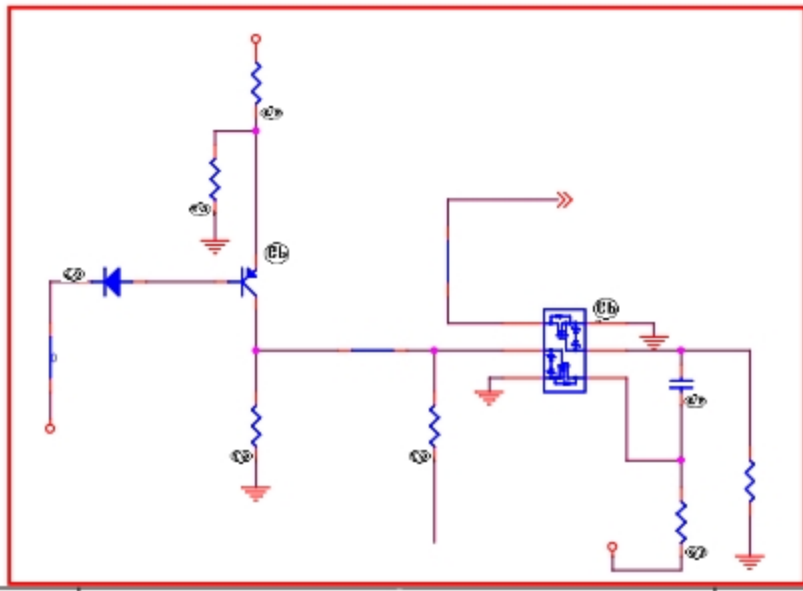
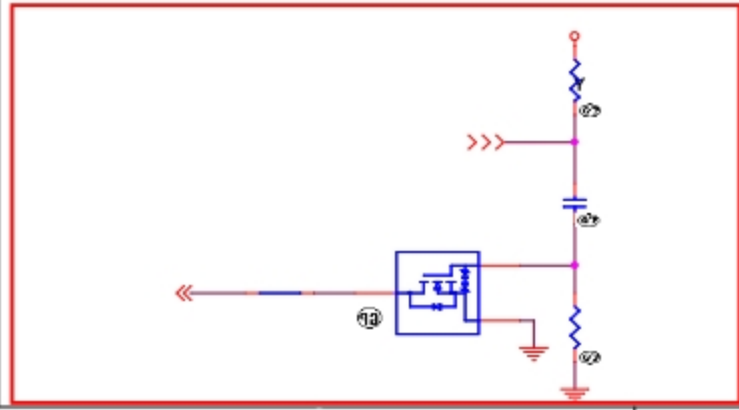


$$I_{CCLIMHW} = \frac{V_{CCLIMHW}}{32 \times PR4436}$$

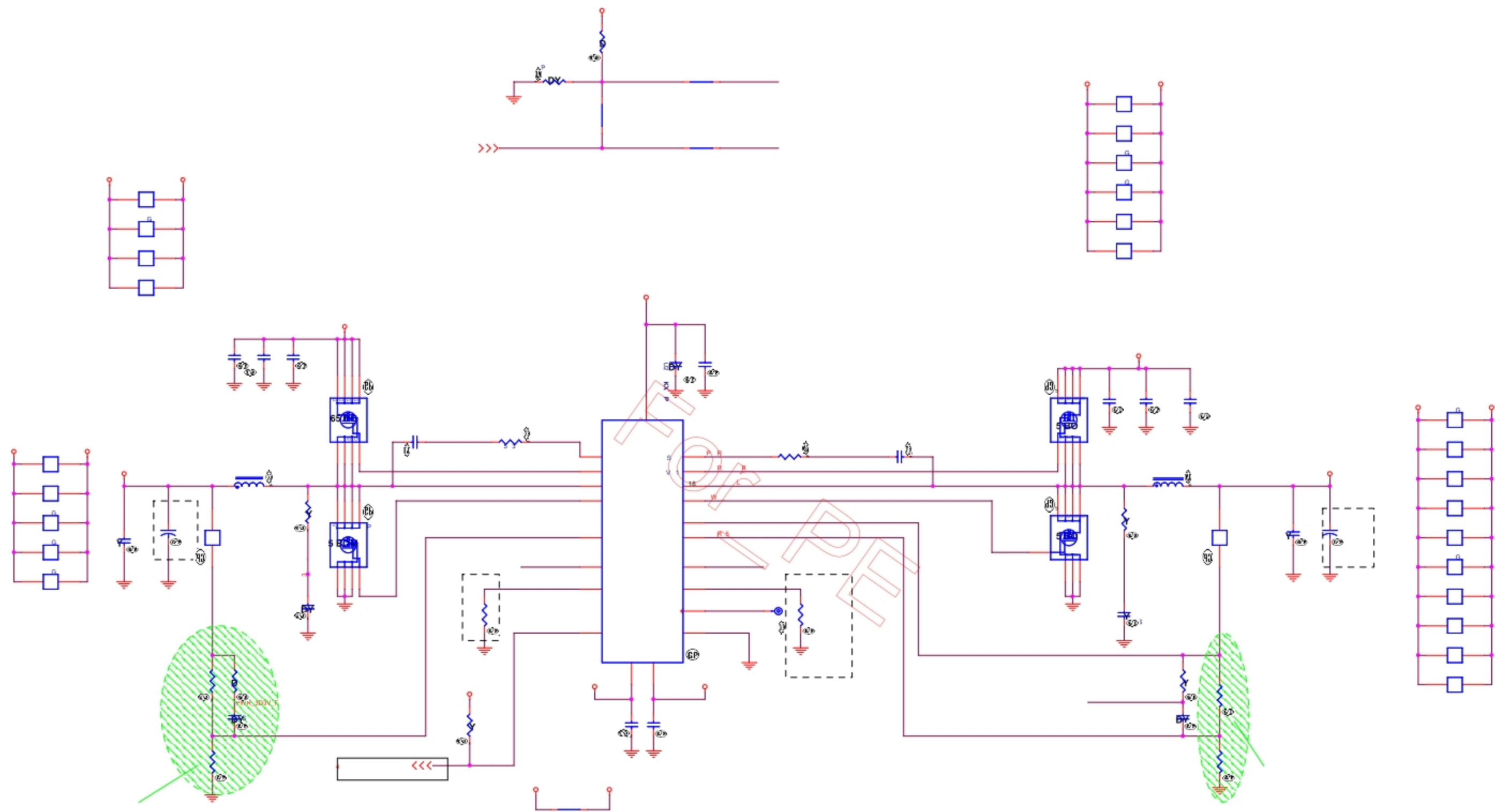
$$I_{ACLIMHW} = \frac{V_{ACLIMHW}}{32 \times PR4433}$$



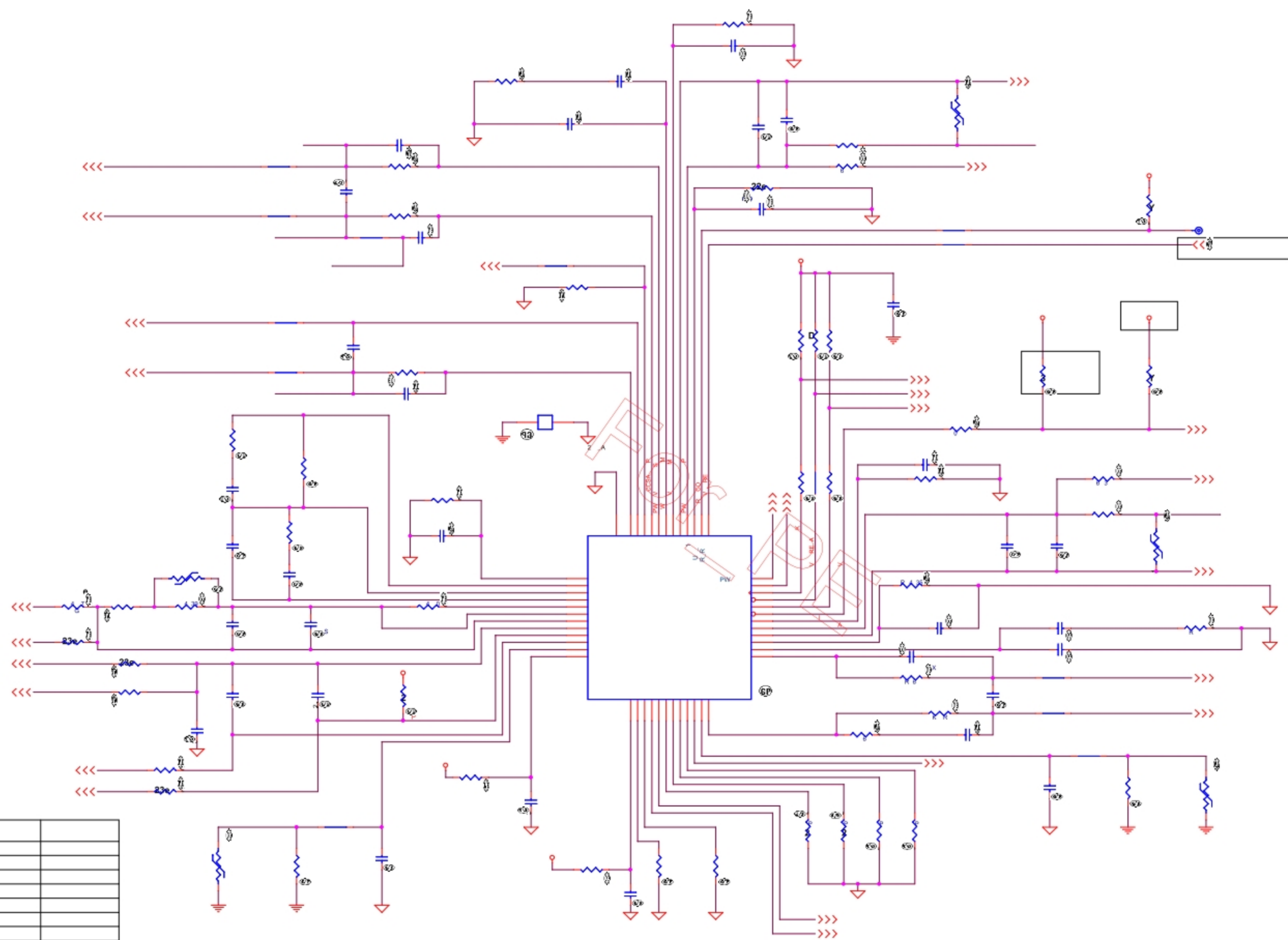
PR4405	2 cell	3 cell	4 cell
NVDC	100k	66.5k	82.5k
HYBRID	165k	182k	147k

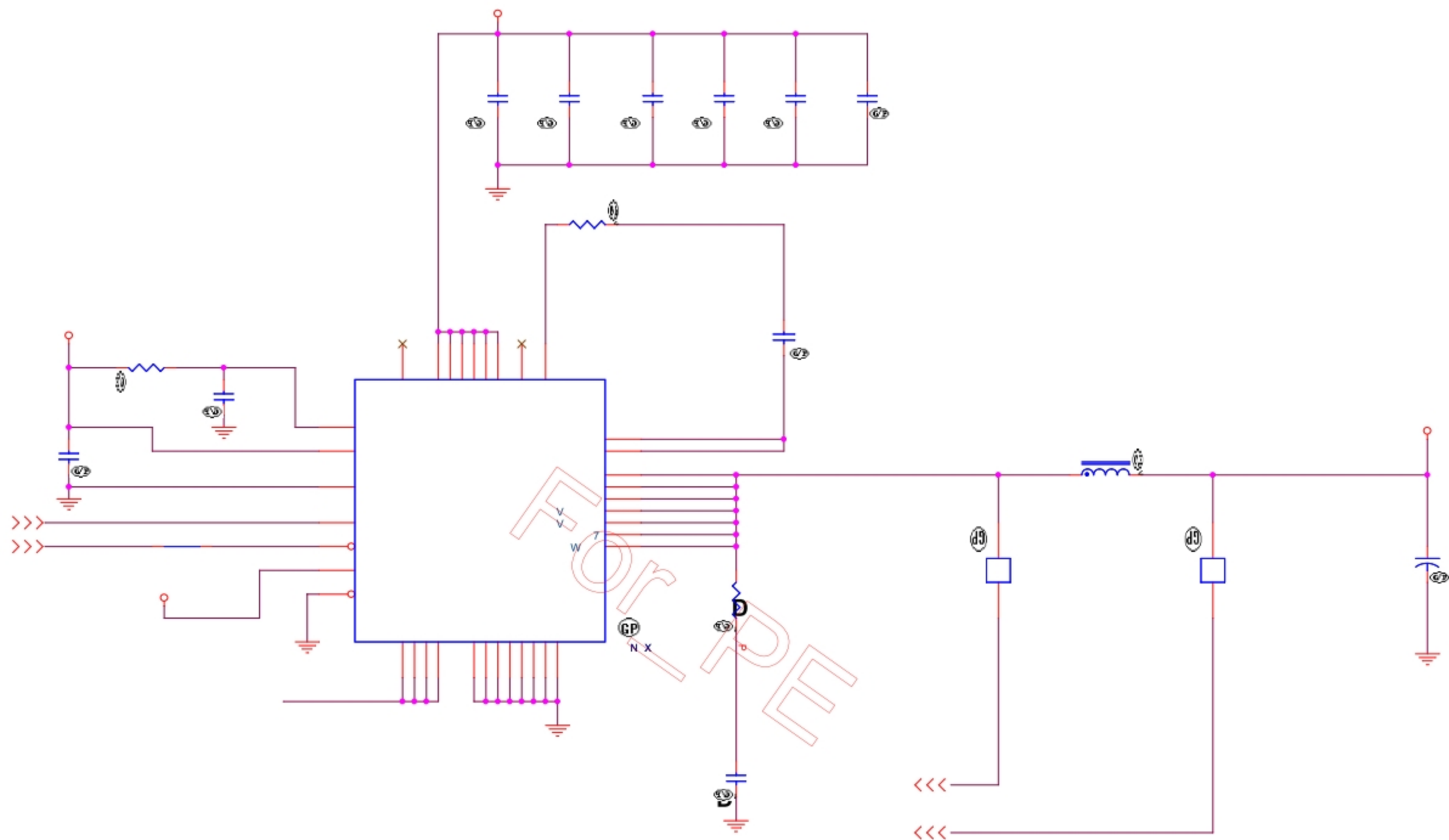


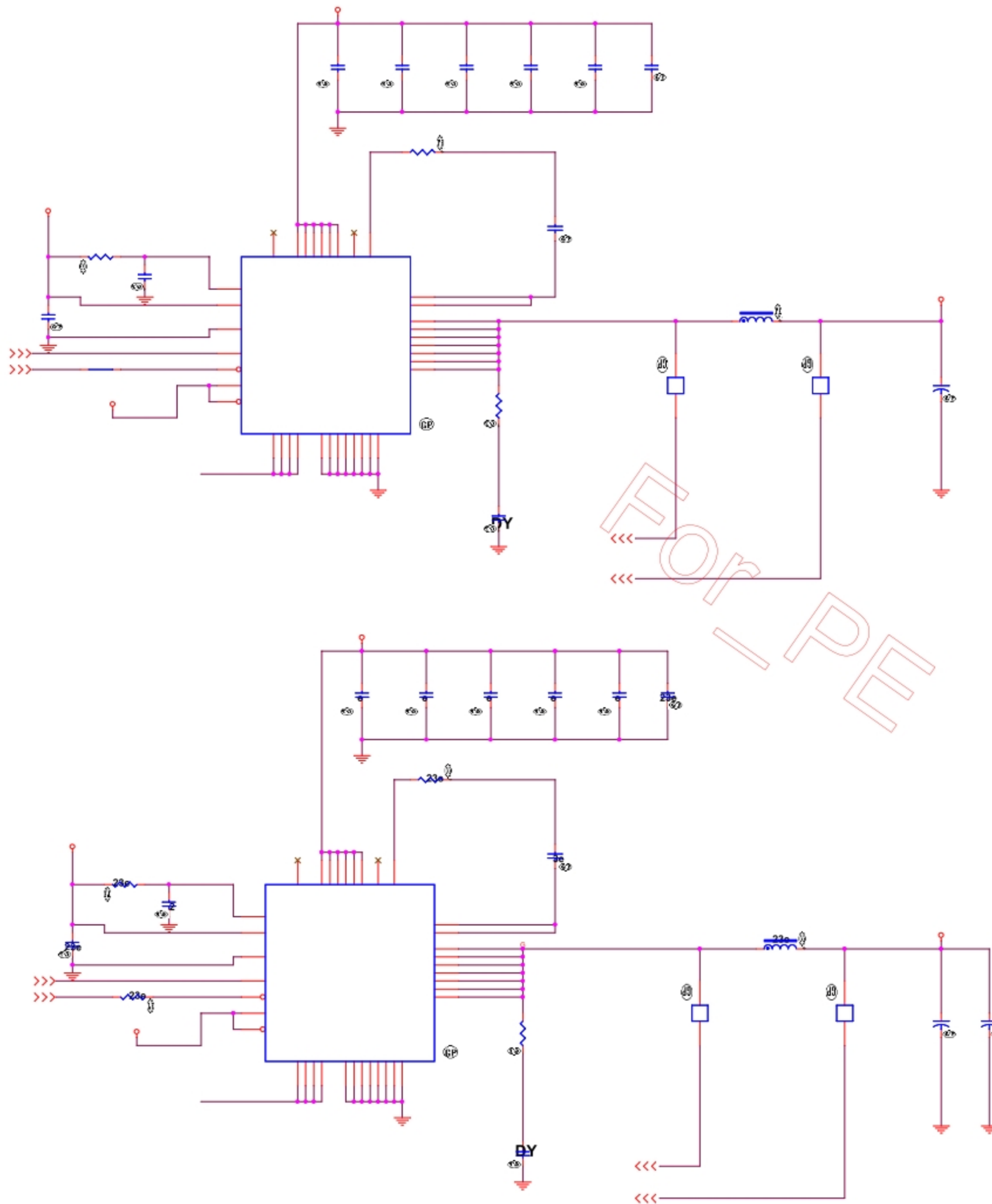




**DELL**

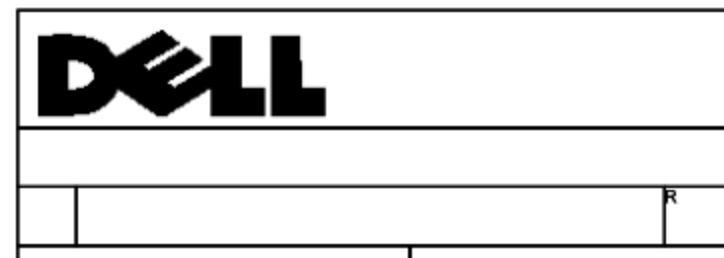
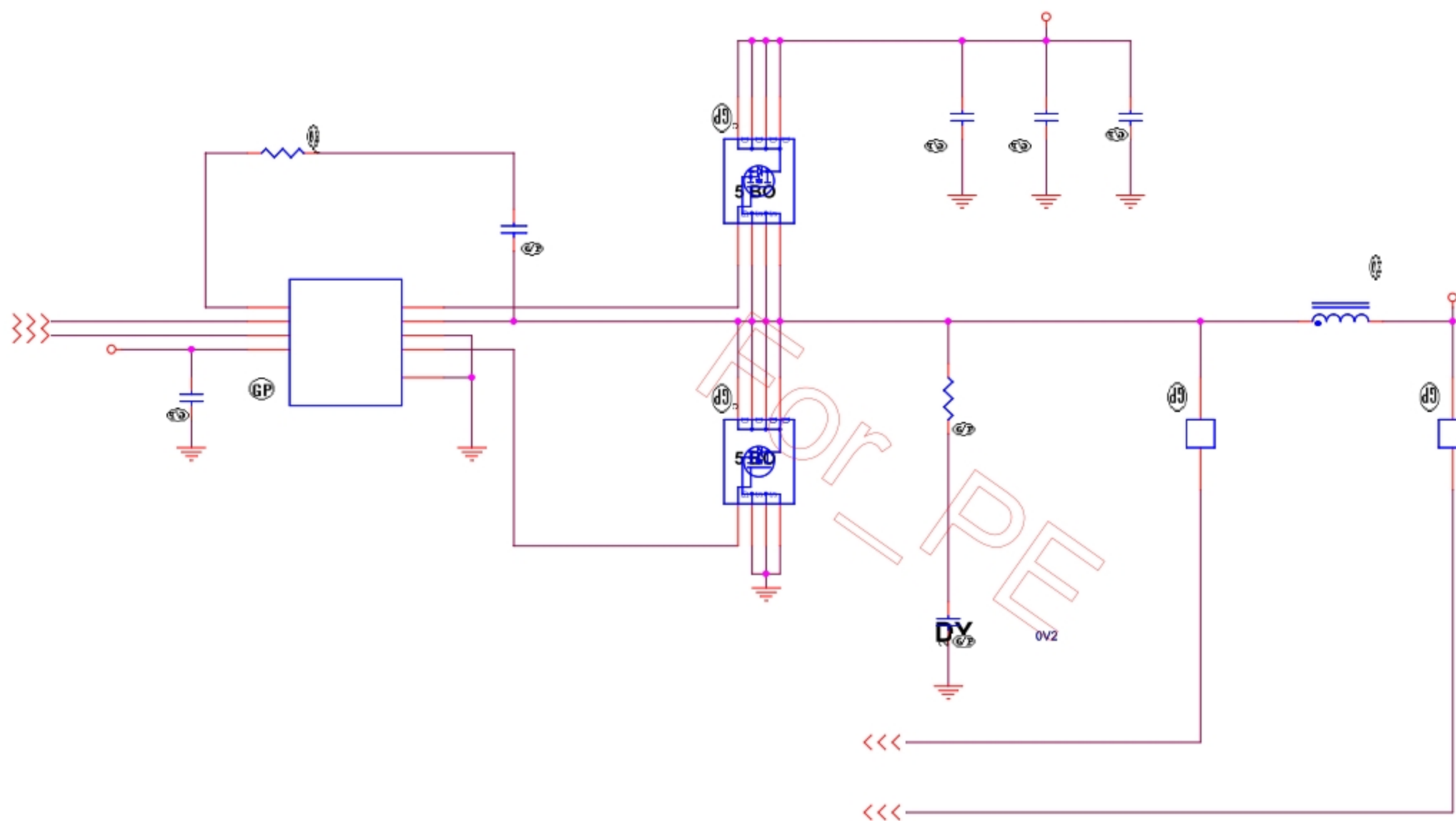



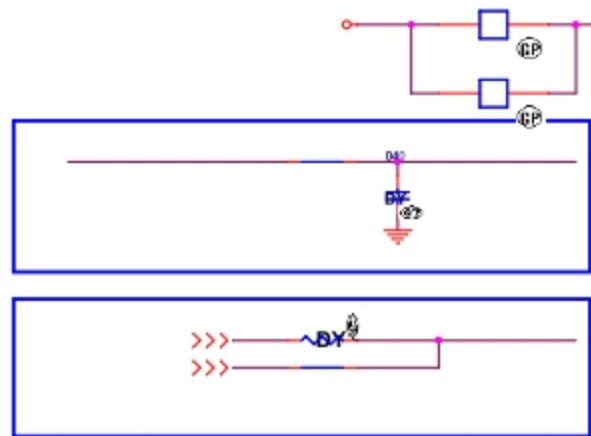
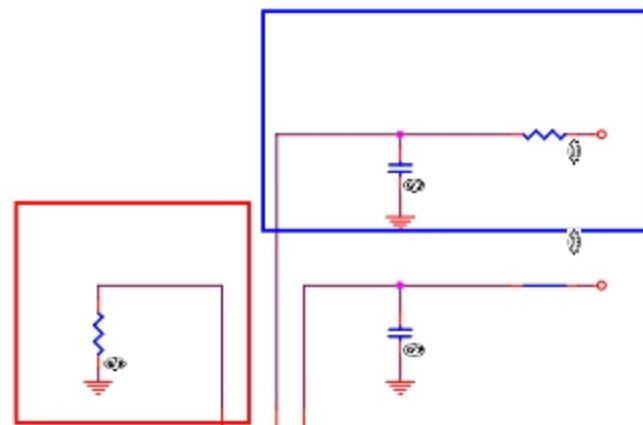
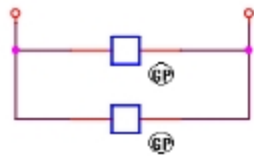





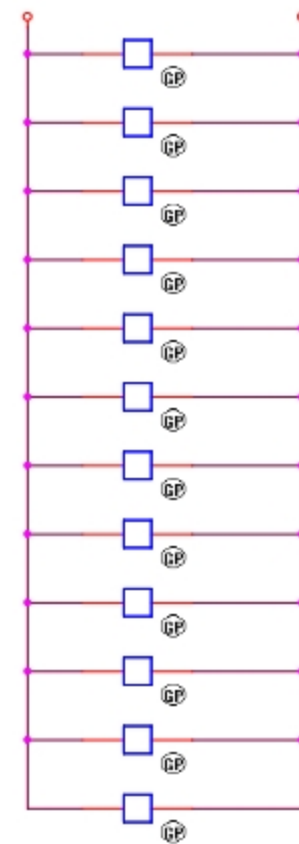
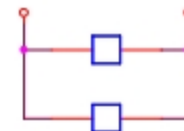
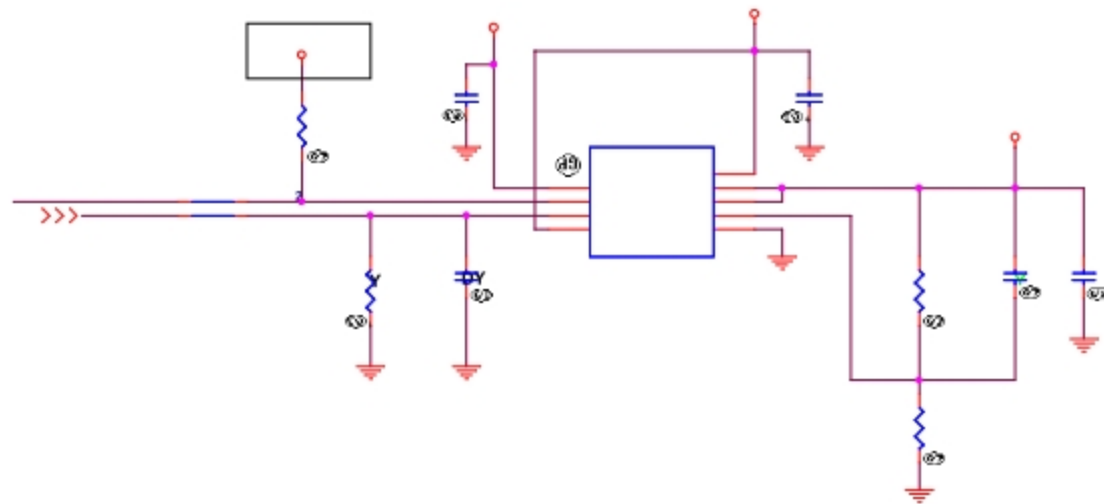
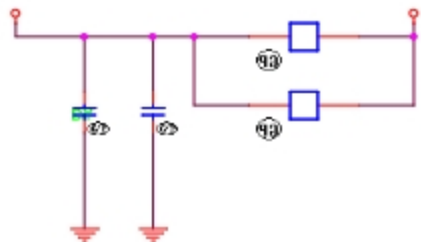
For PE

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State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

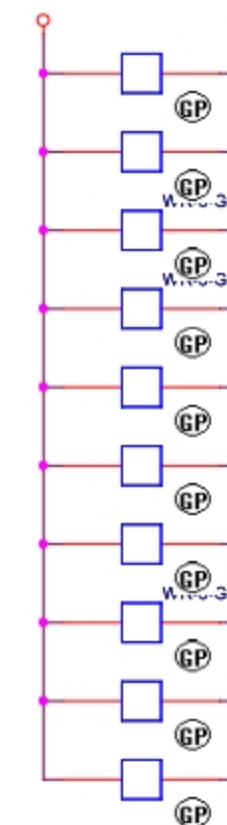
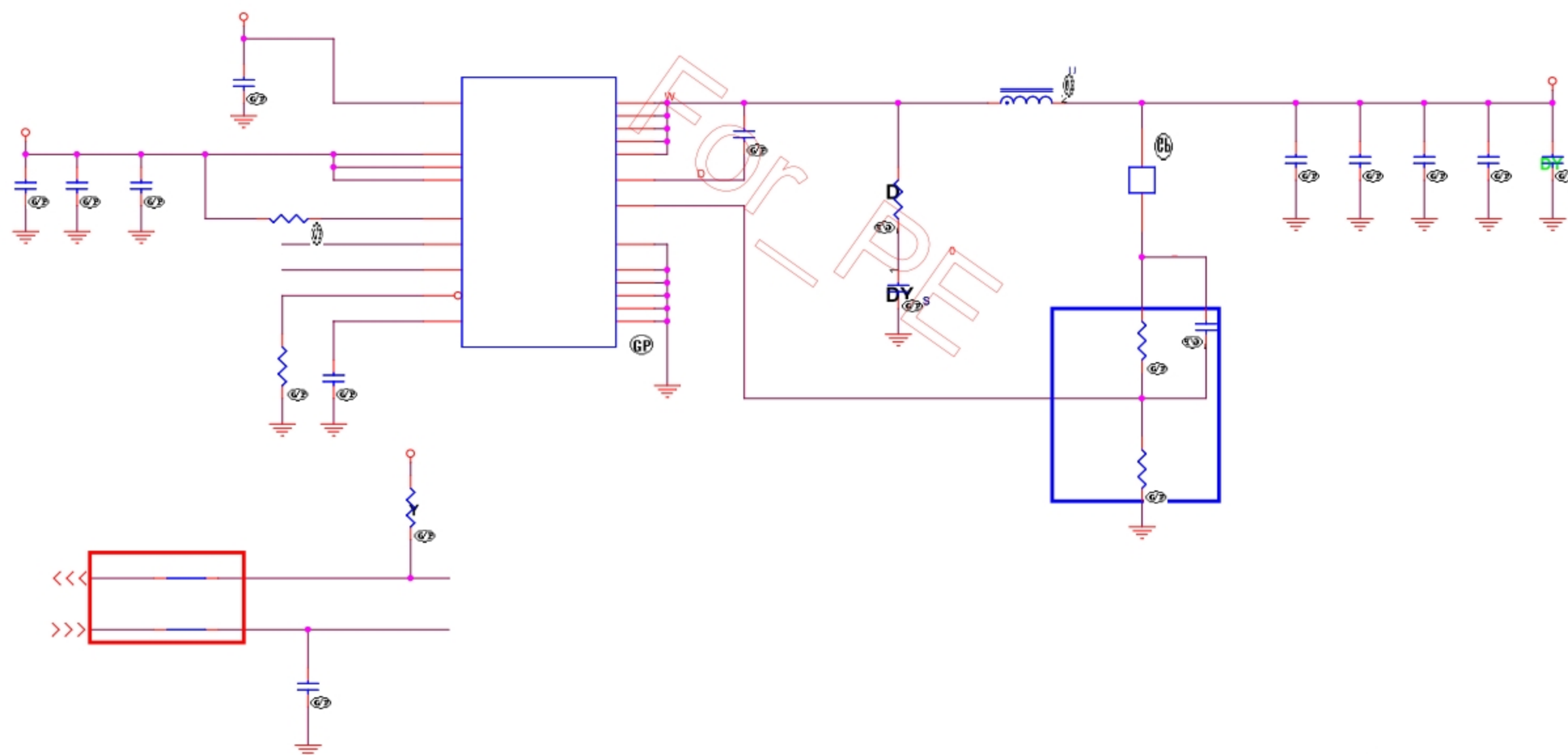
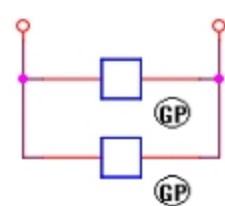


For PE

**DELL**

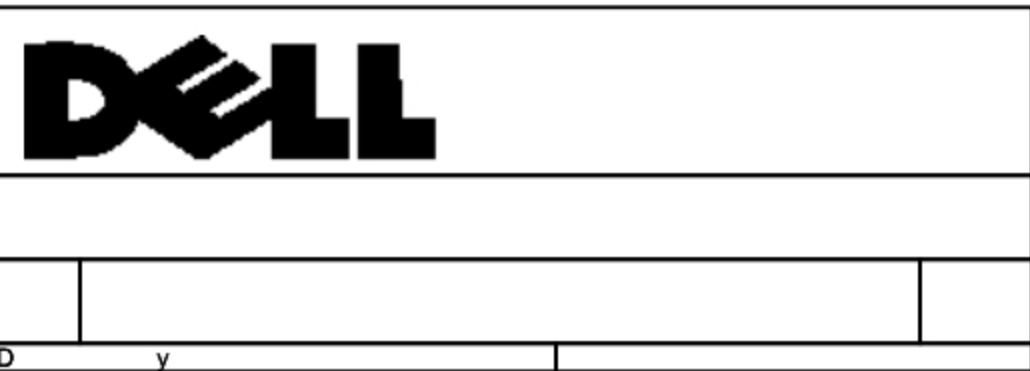
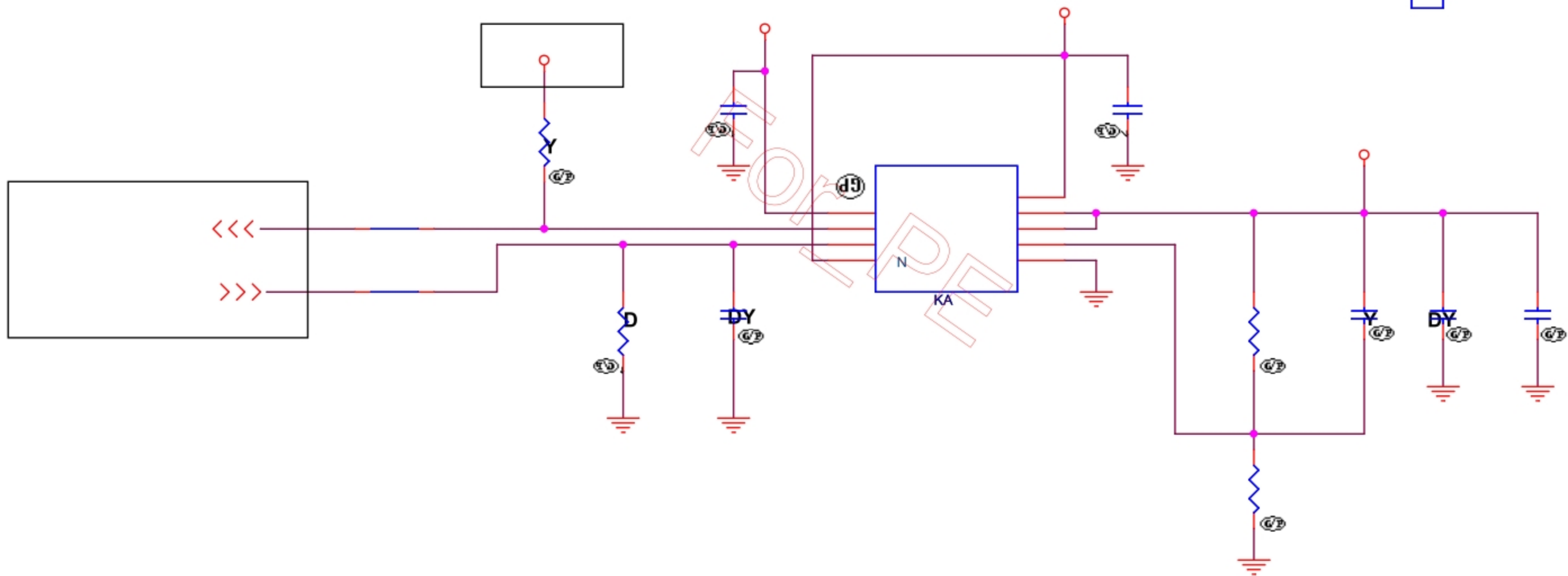
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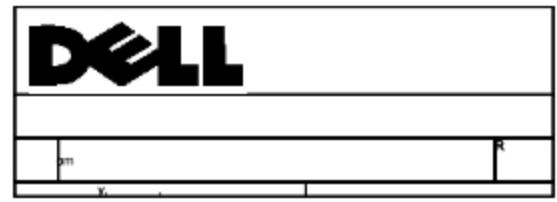
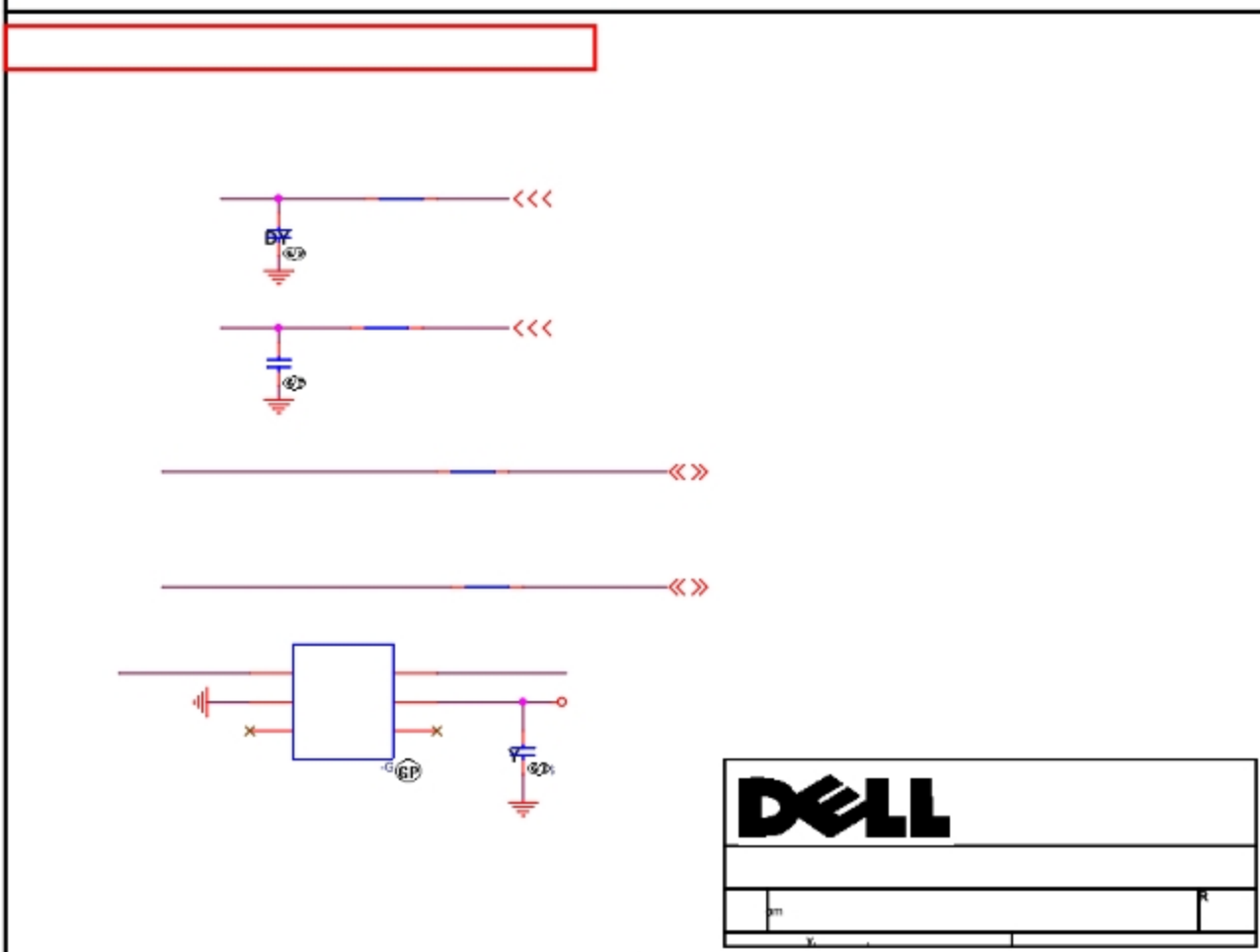
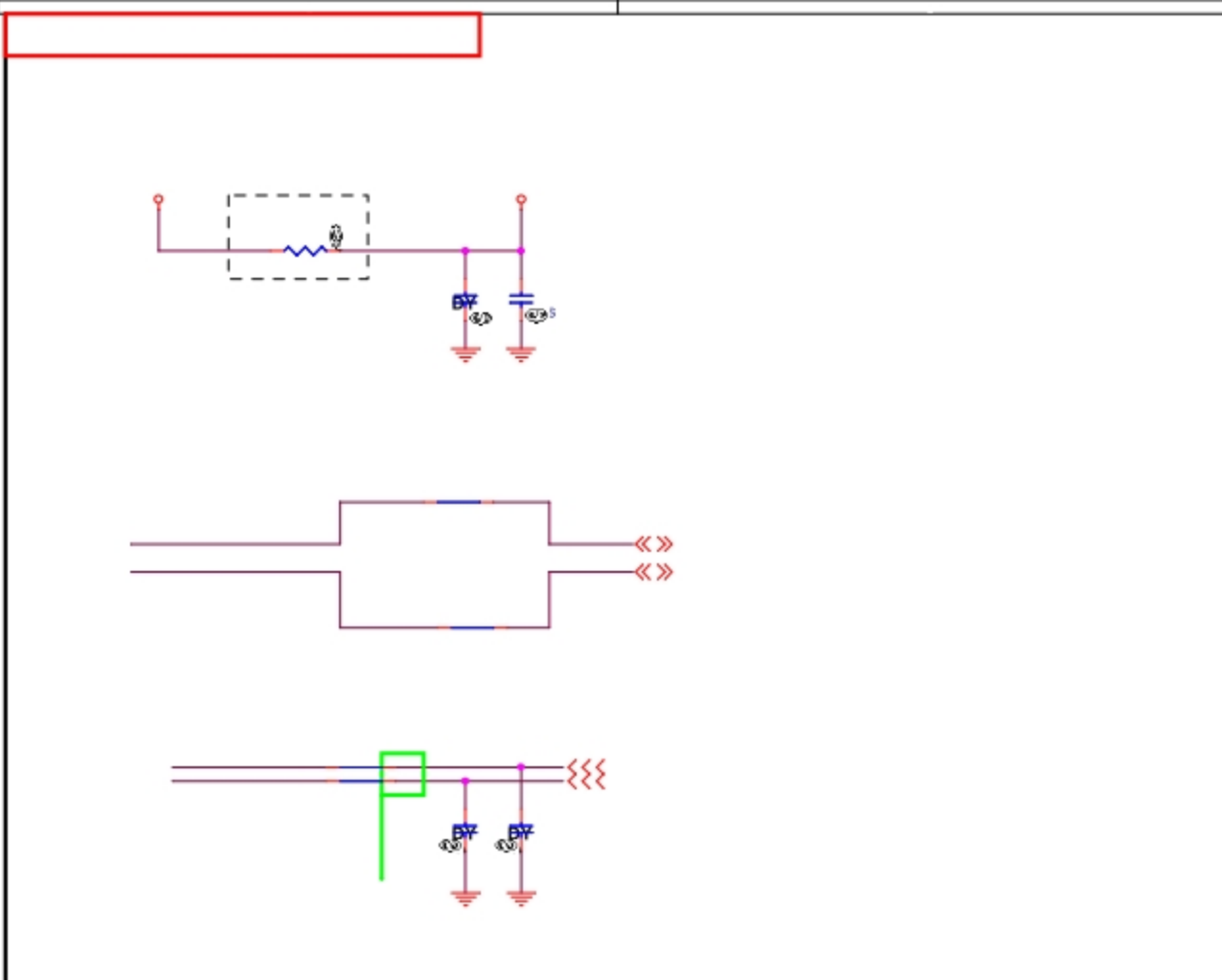
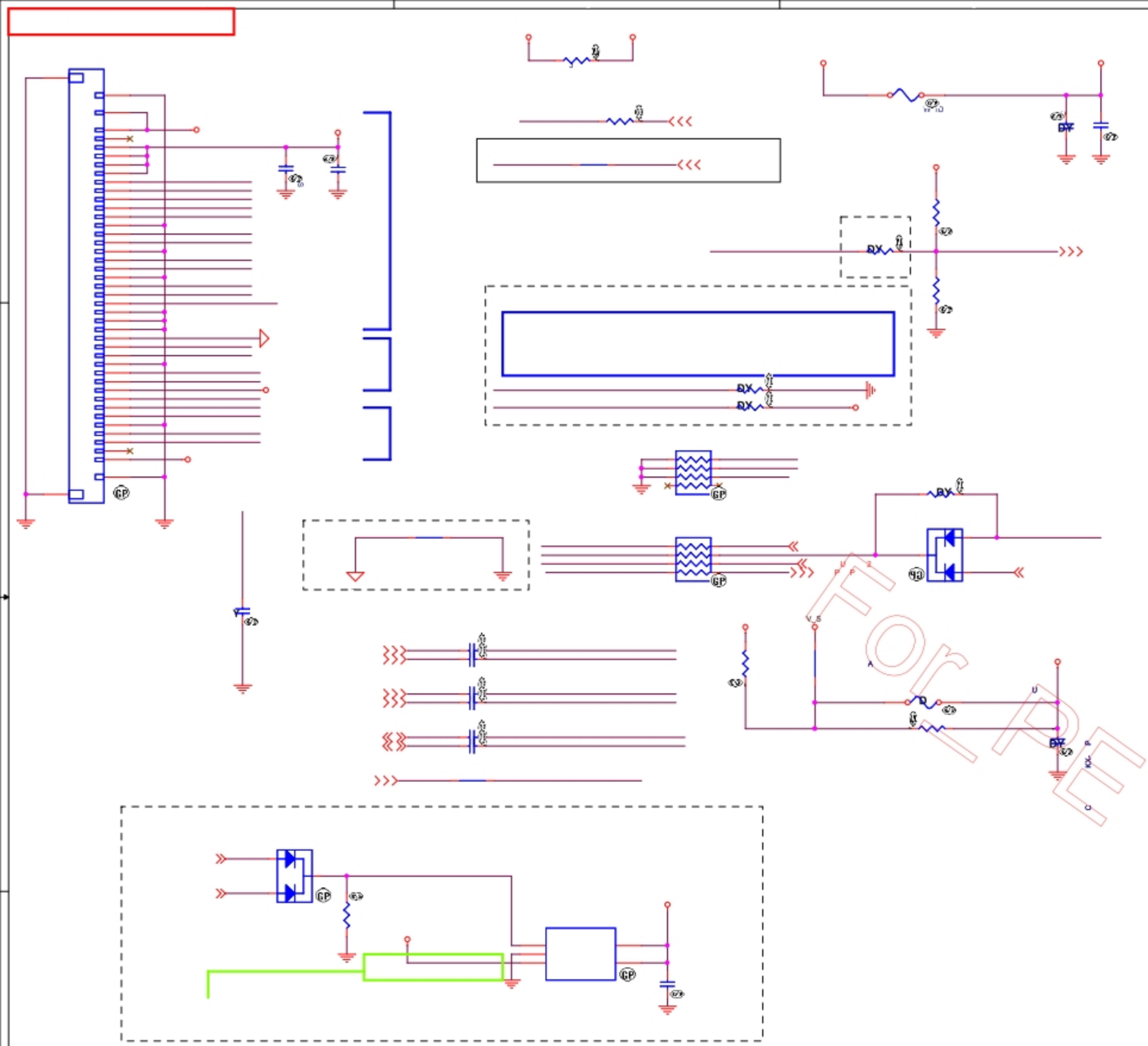


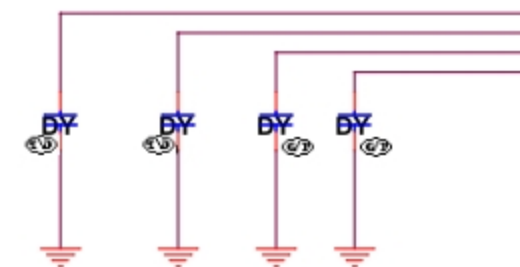
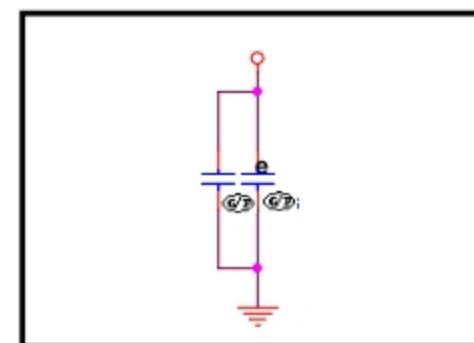
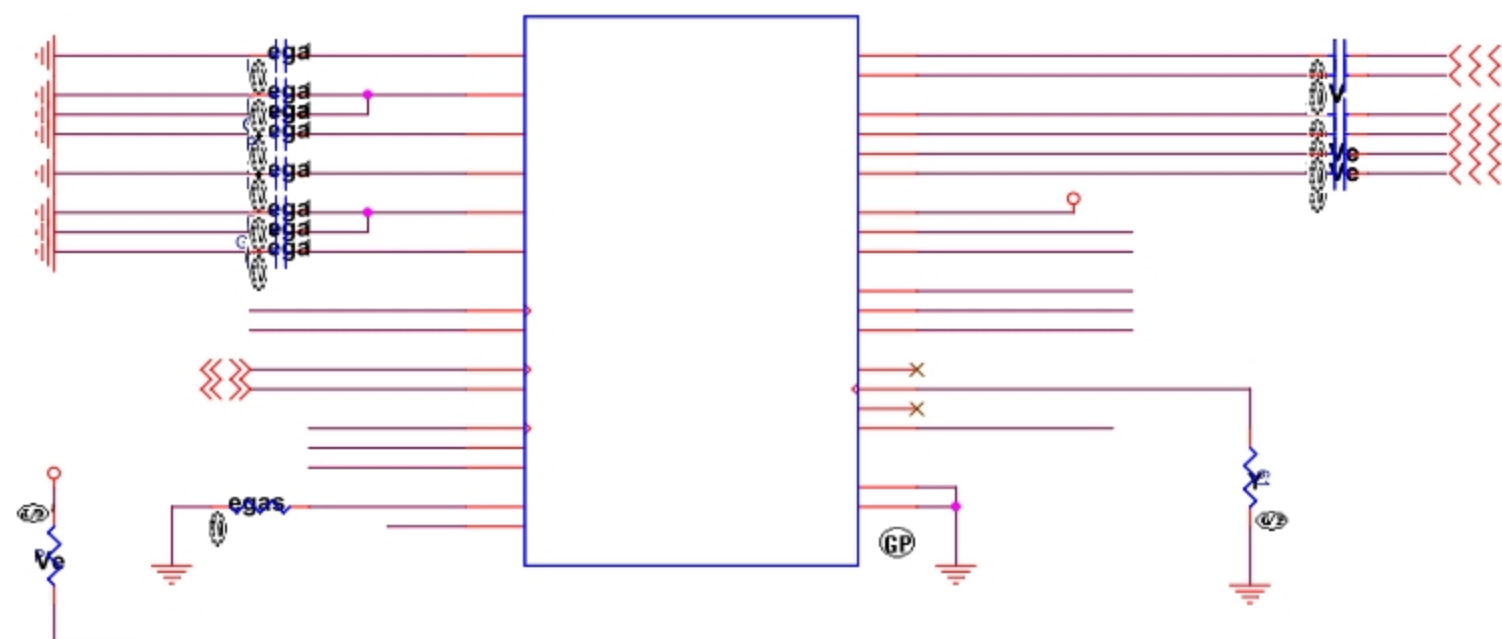
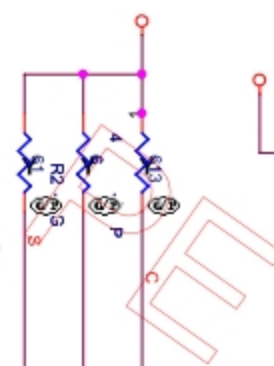
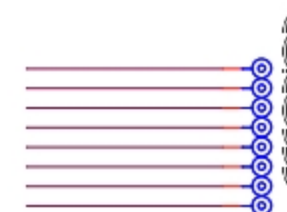
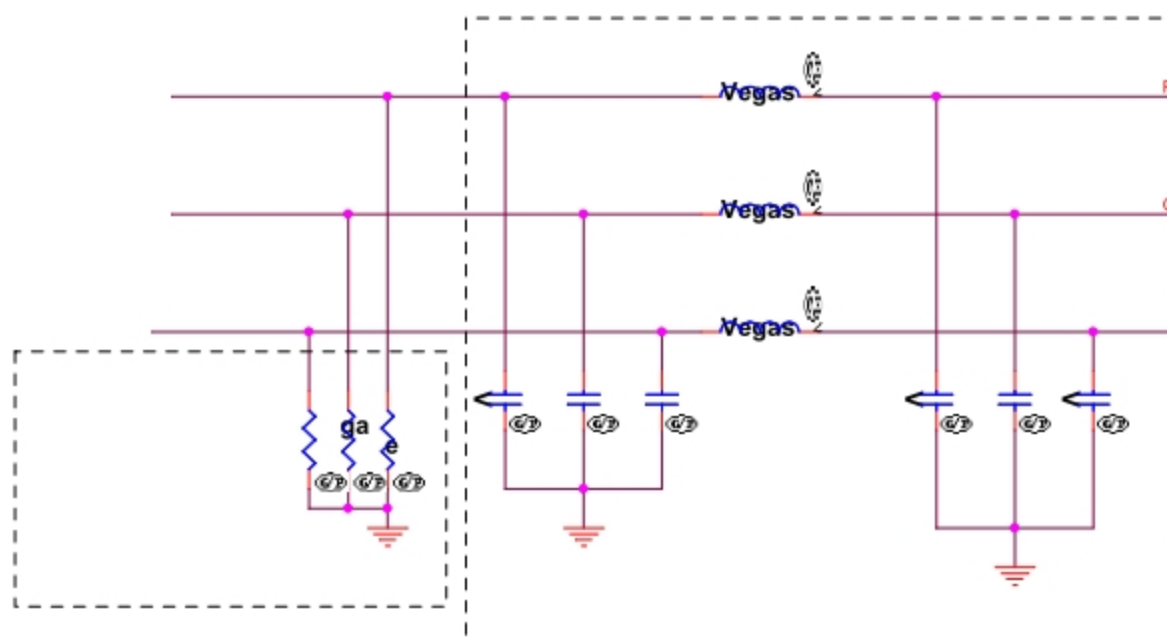
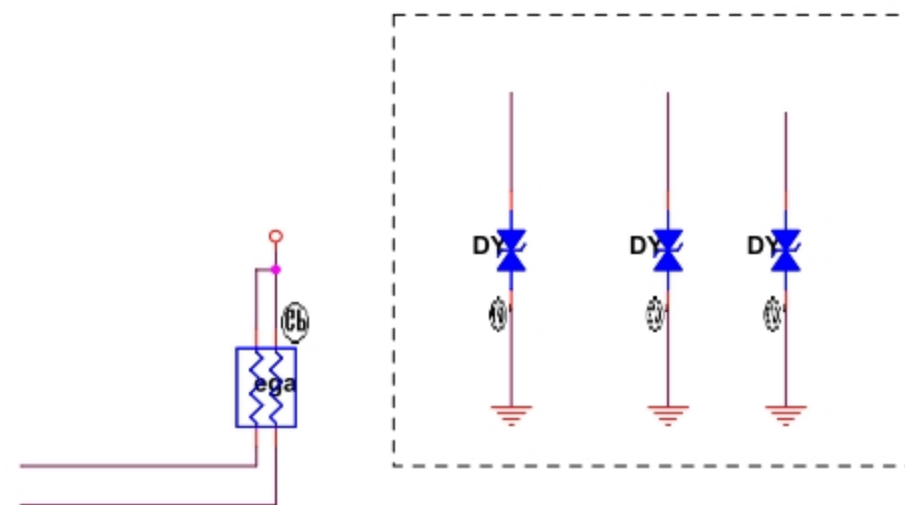
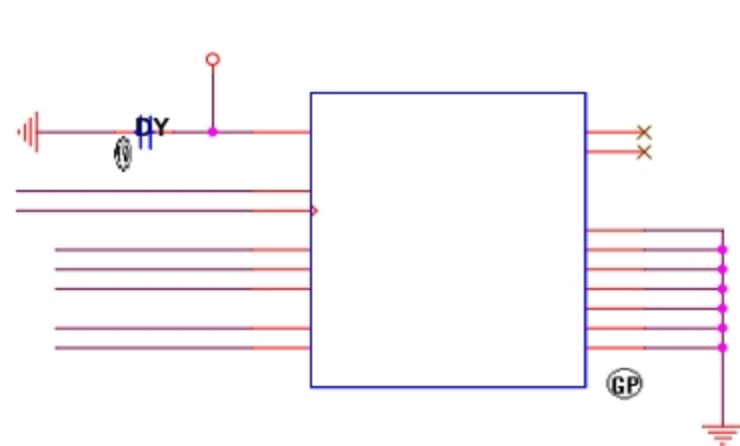


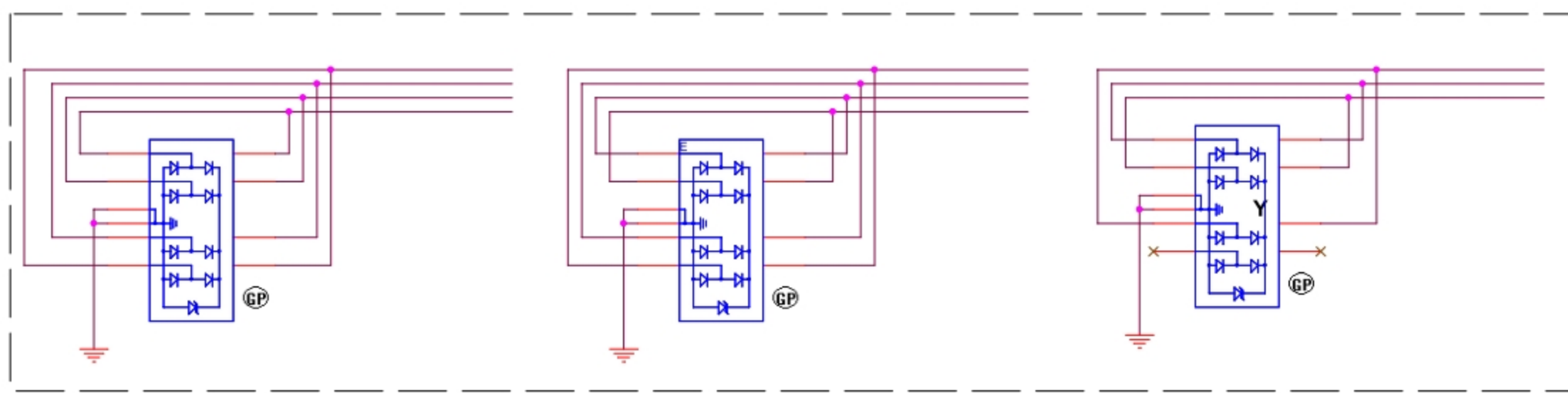
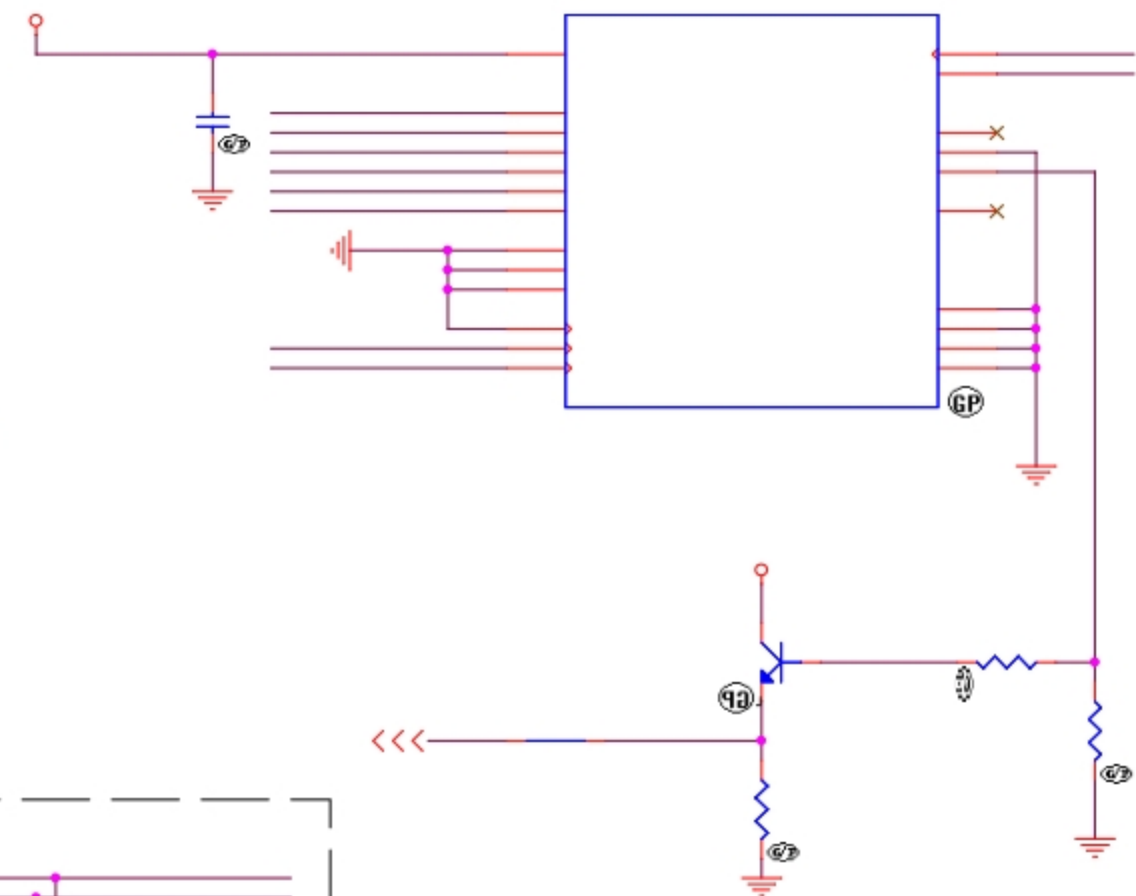
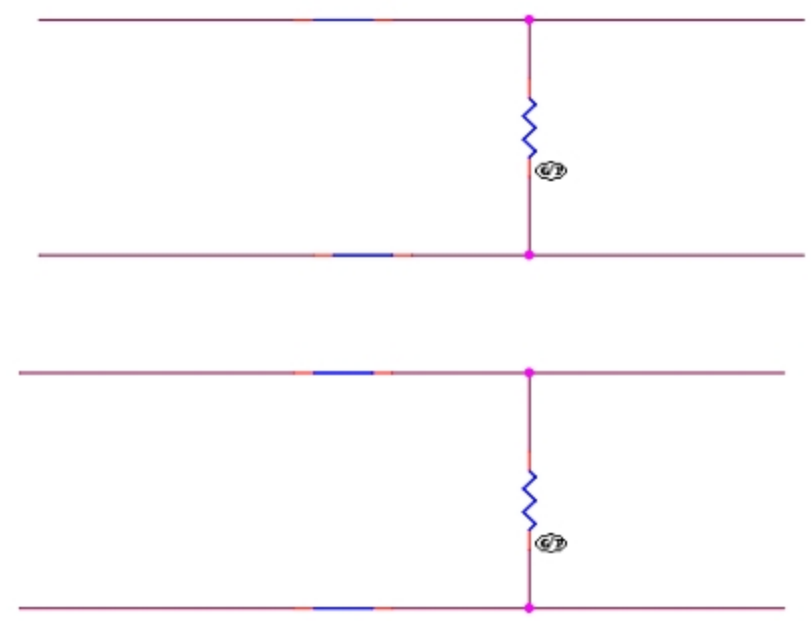
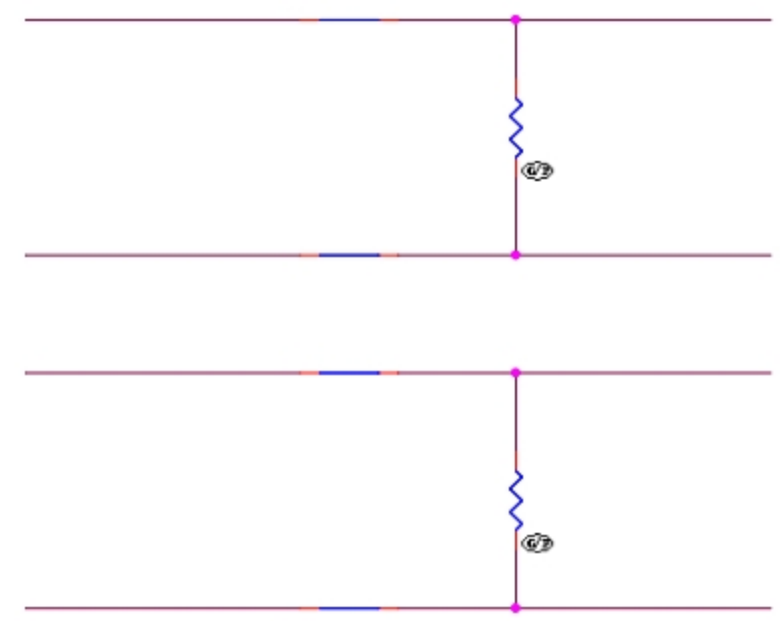
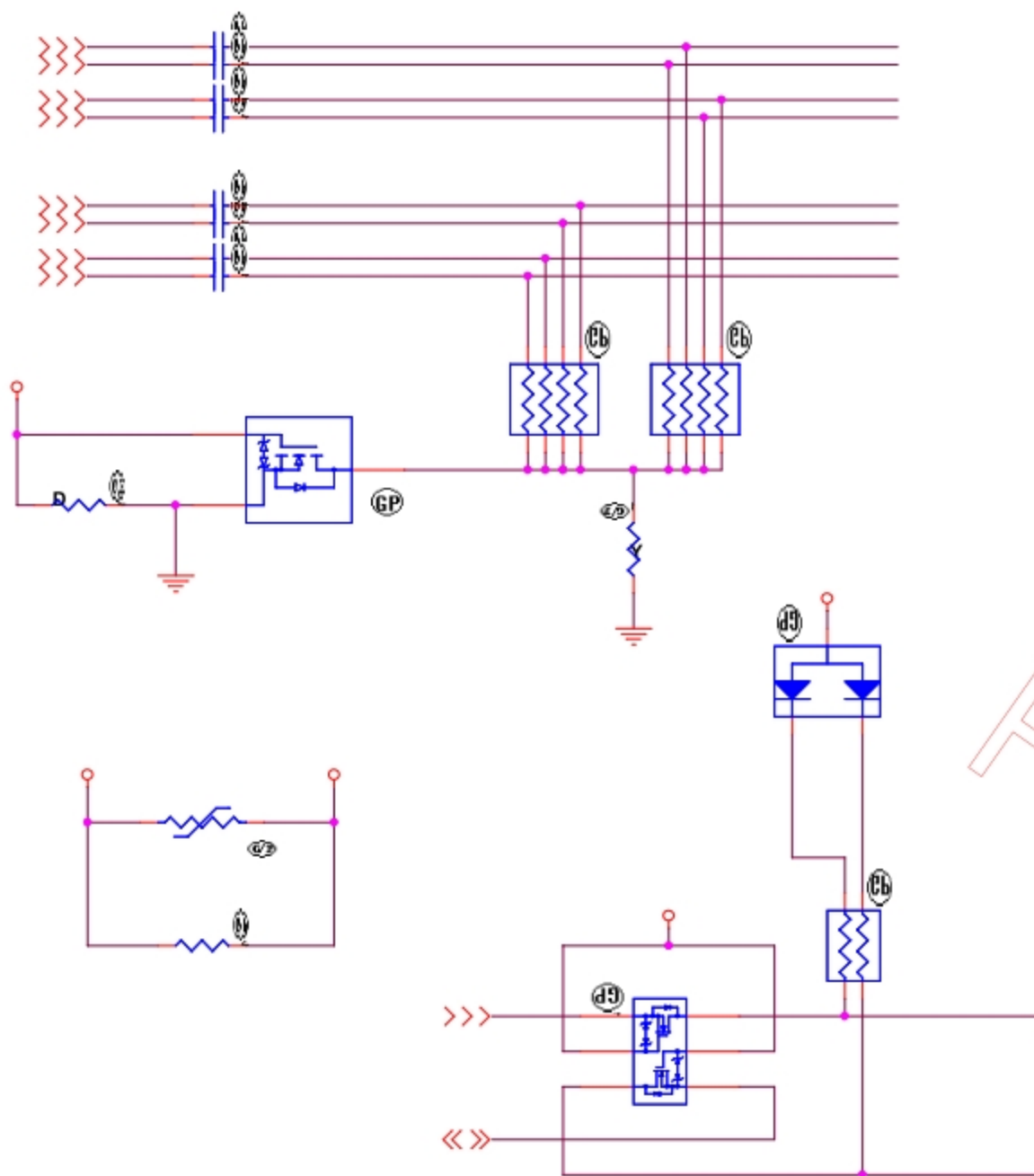
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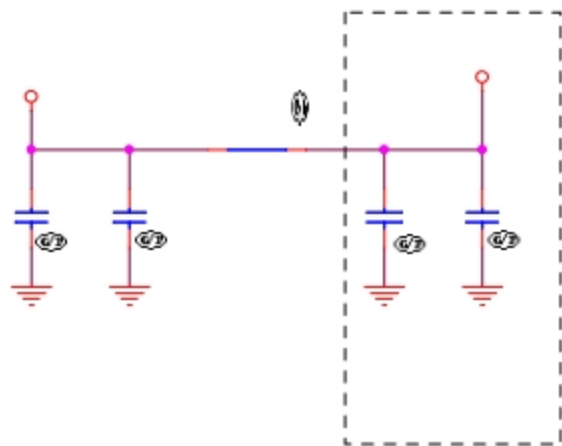


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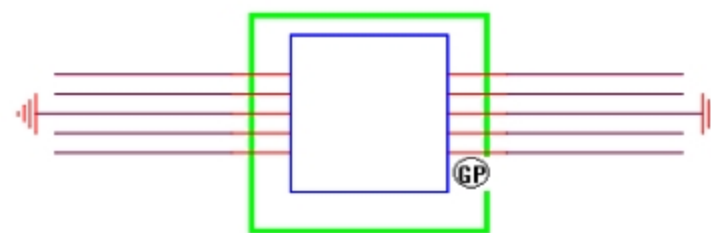
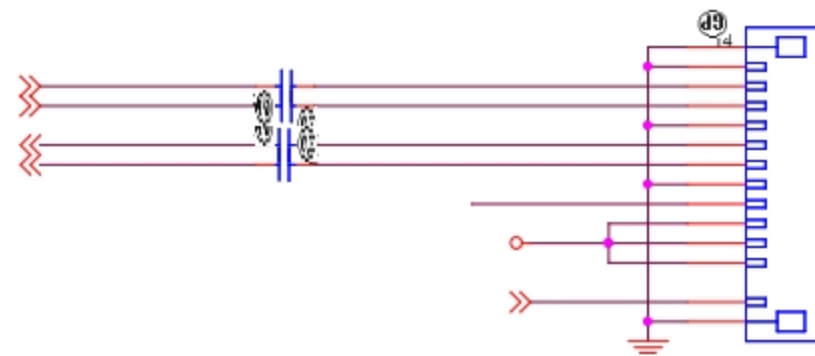
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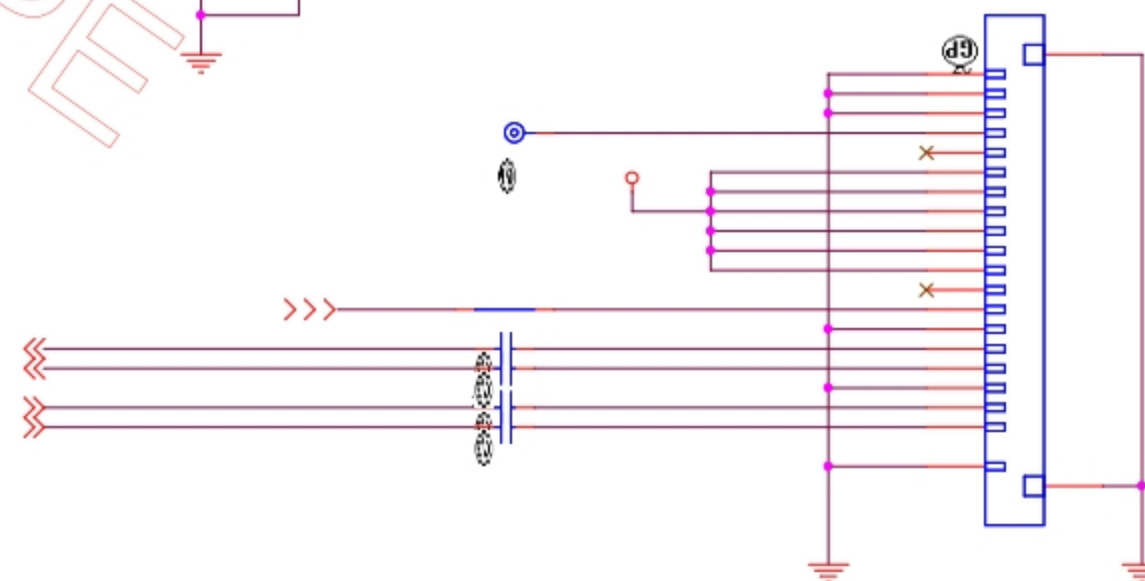
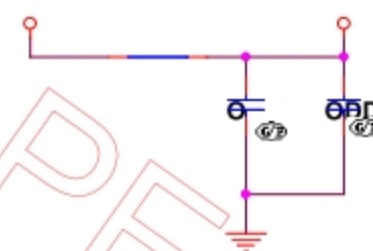
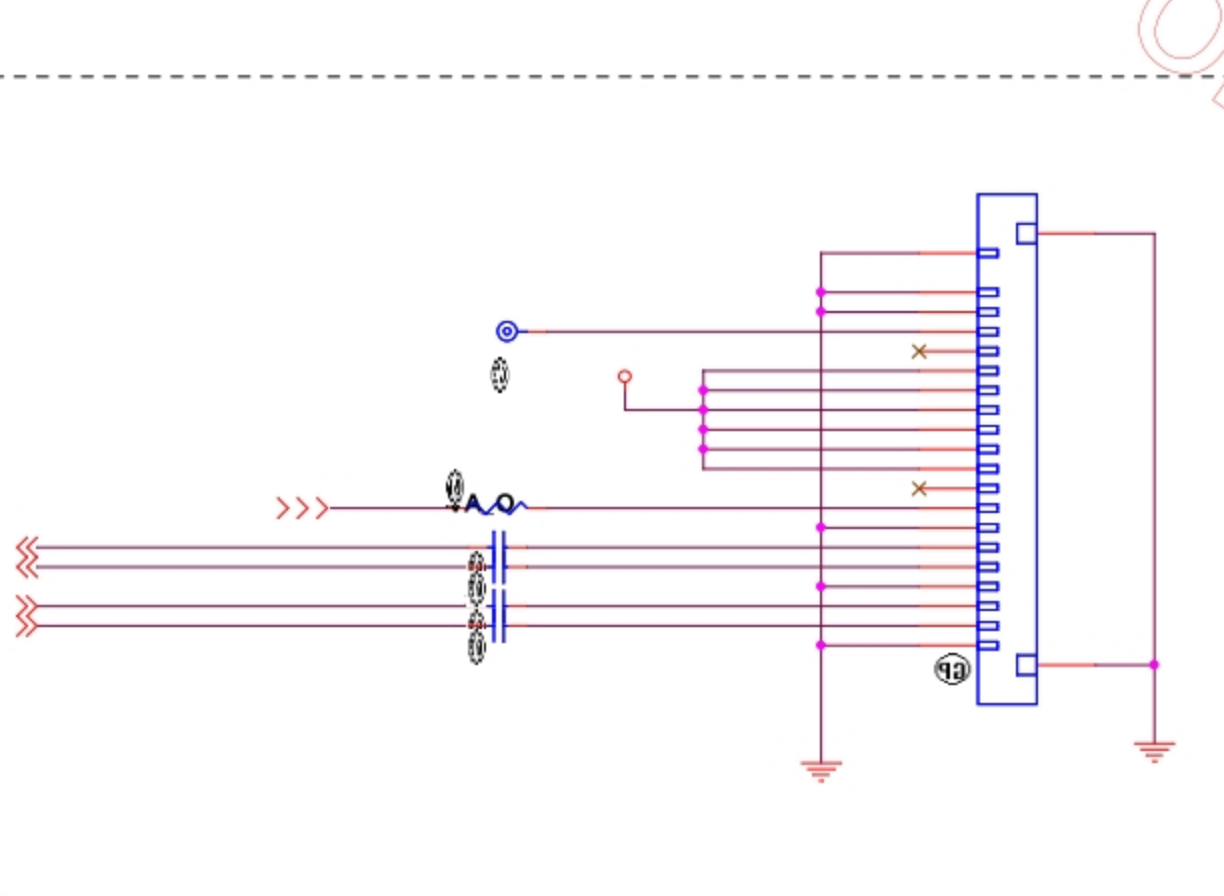


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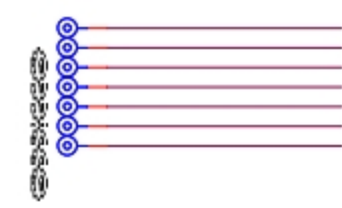
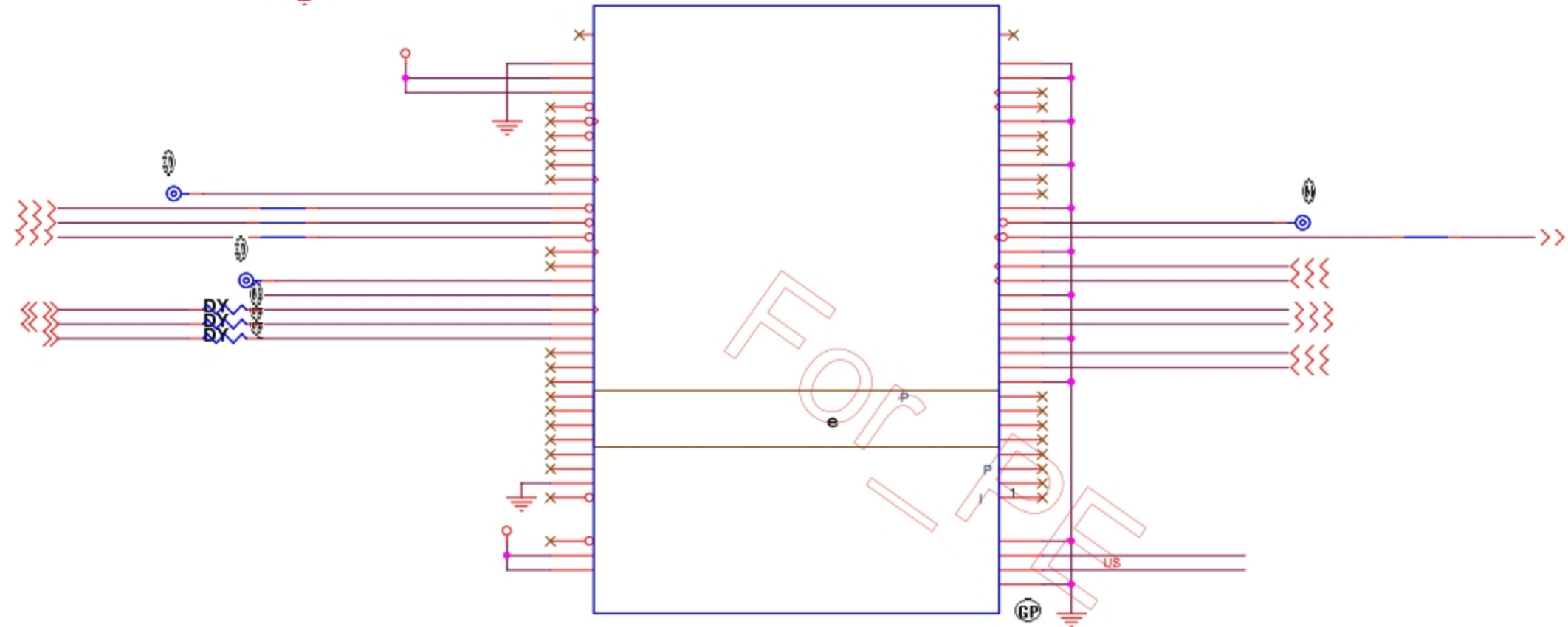
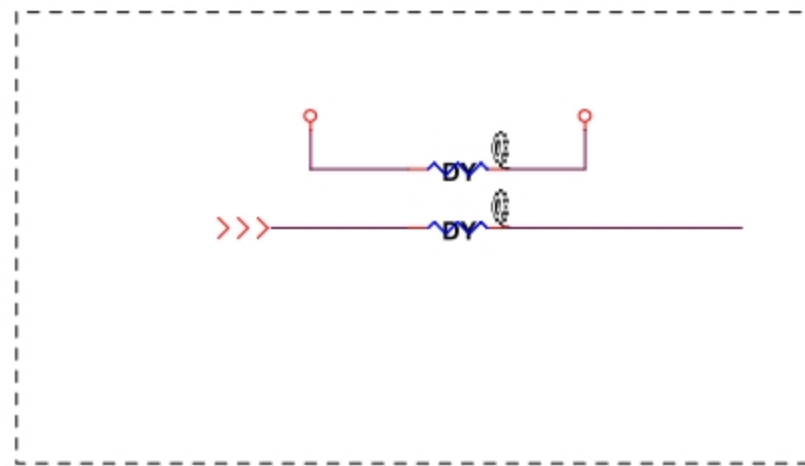
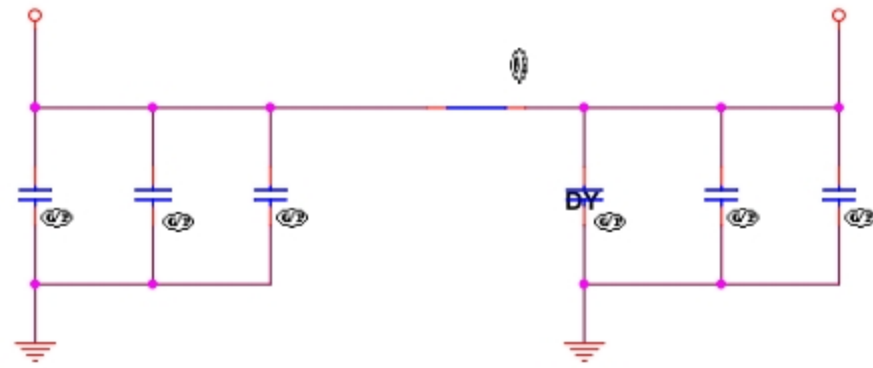
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CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	



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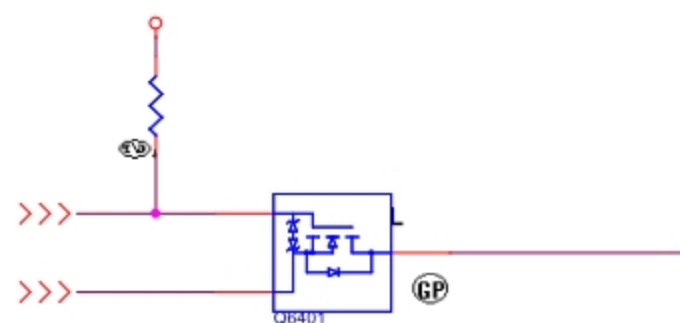
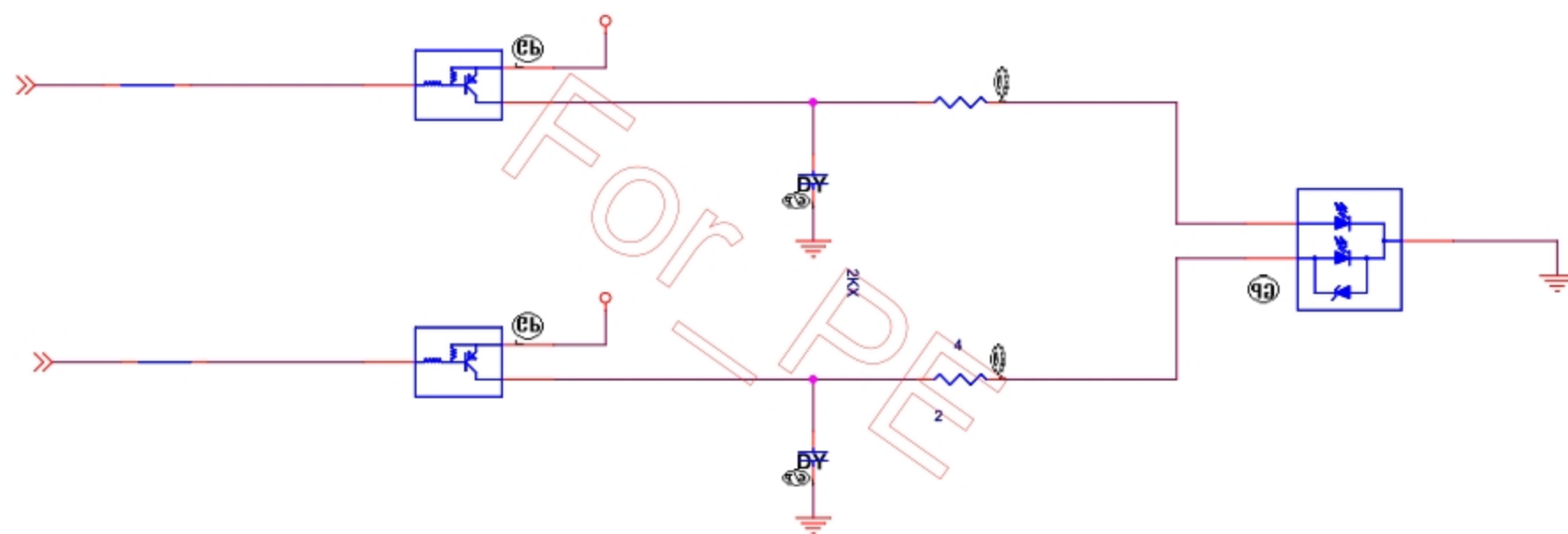
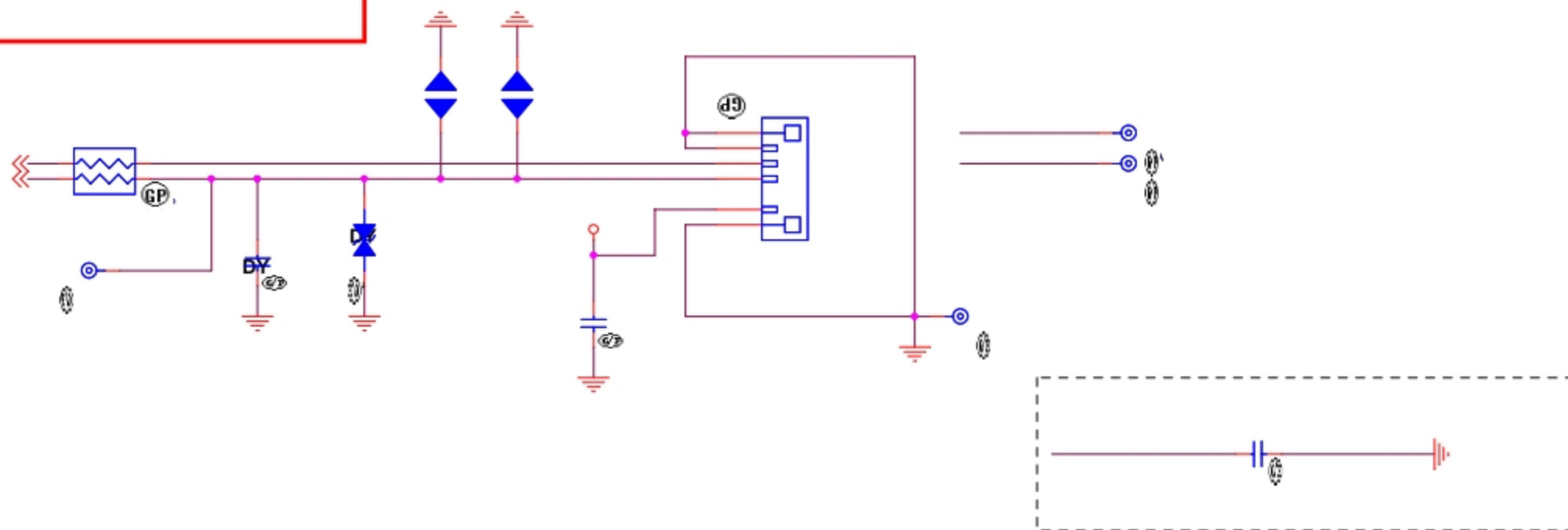
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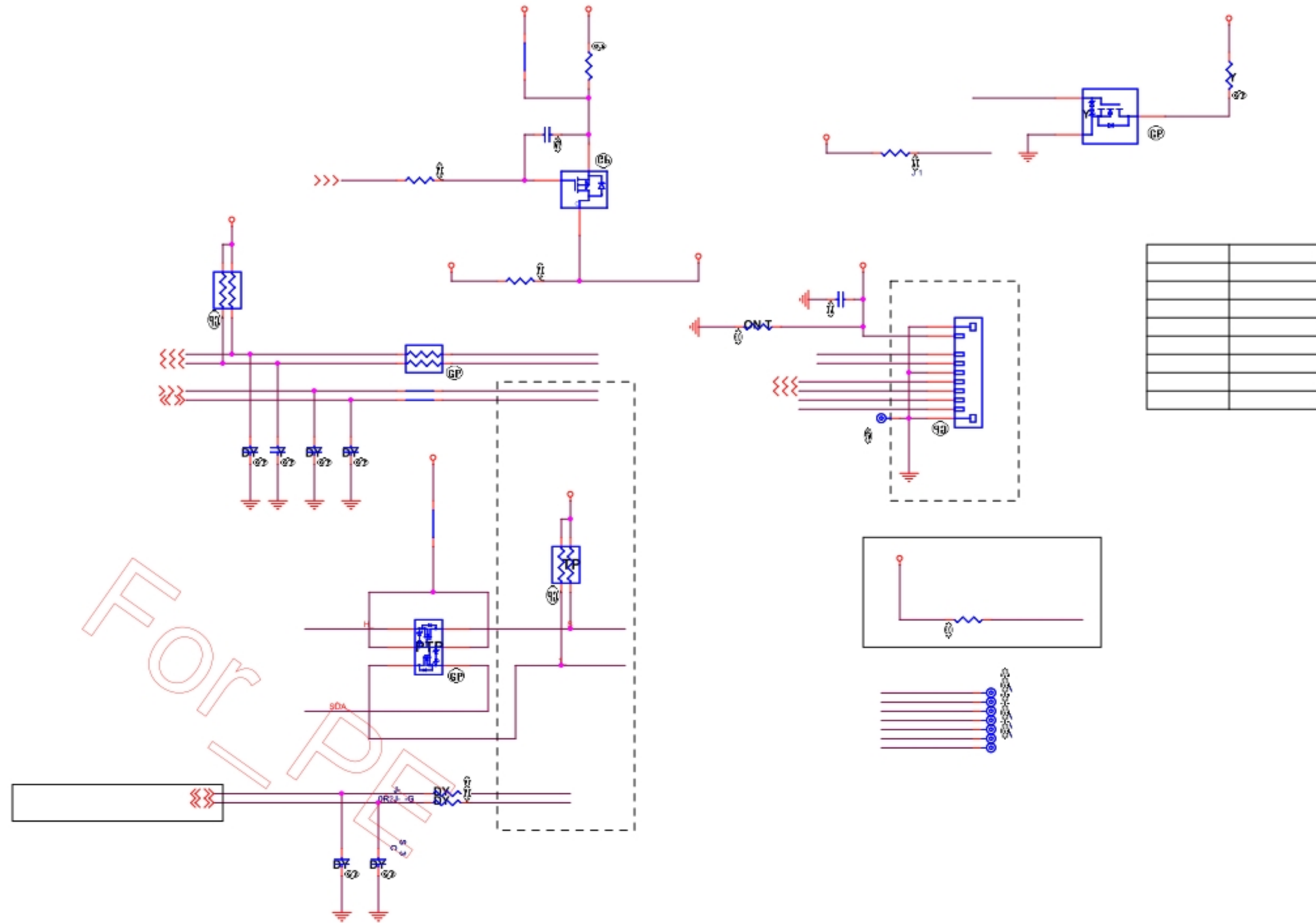
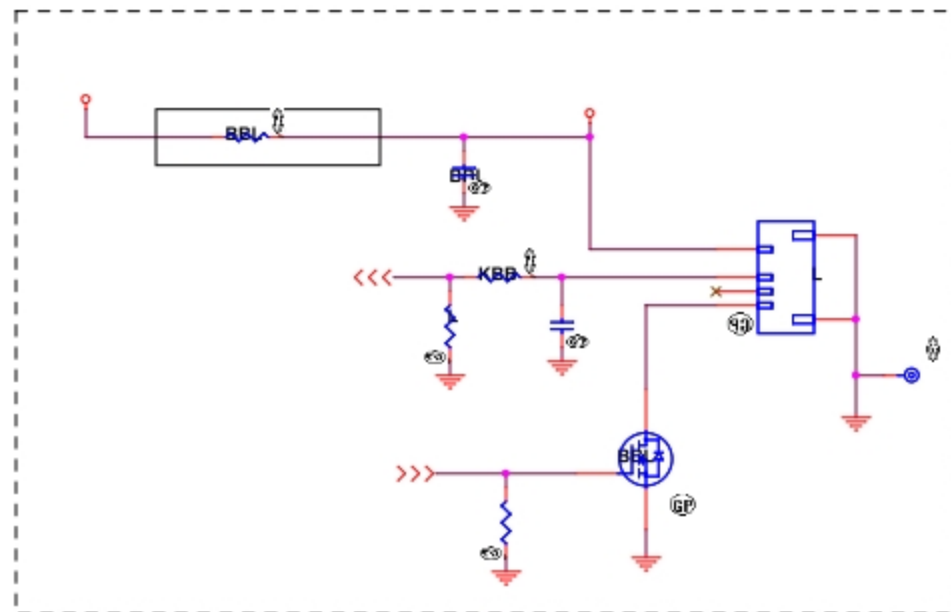
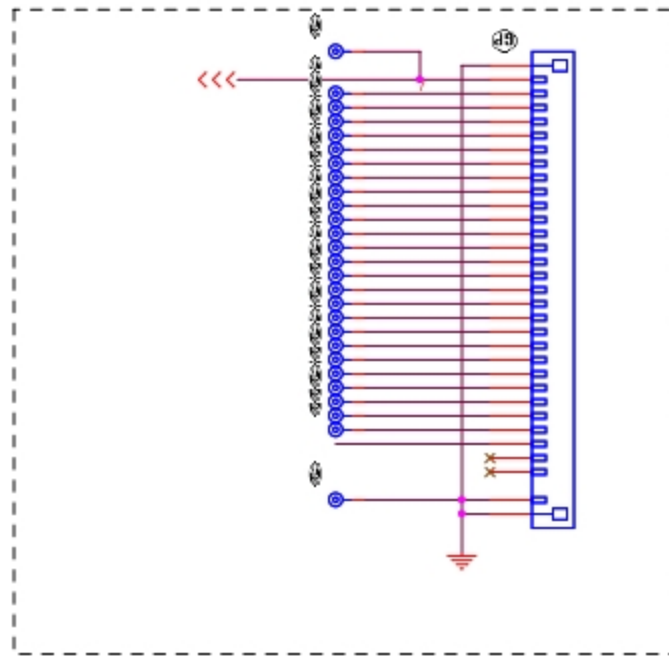
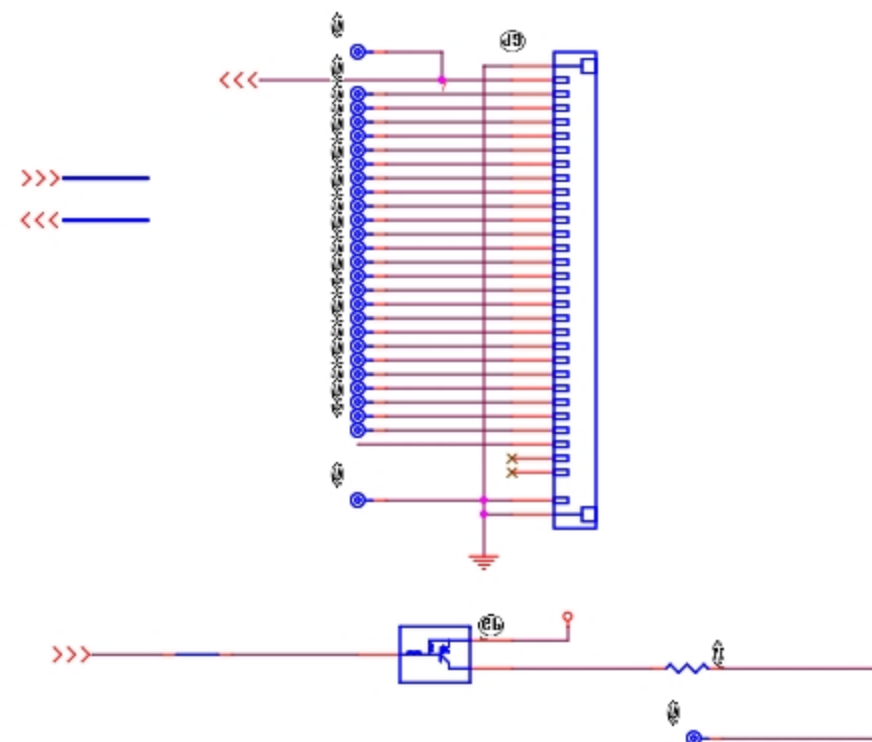
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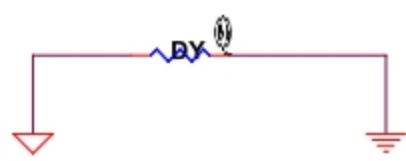
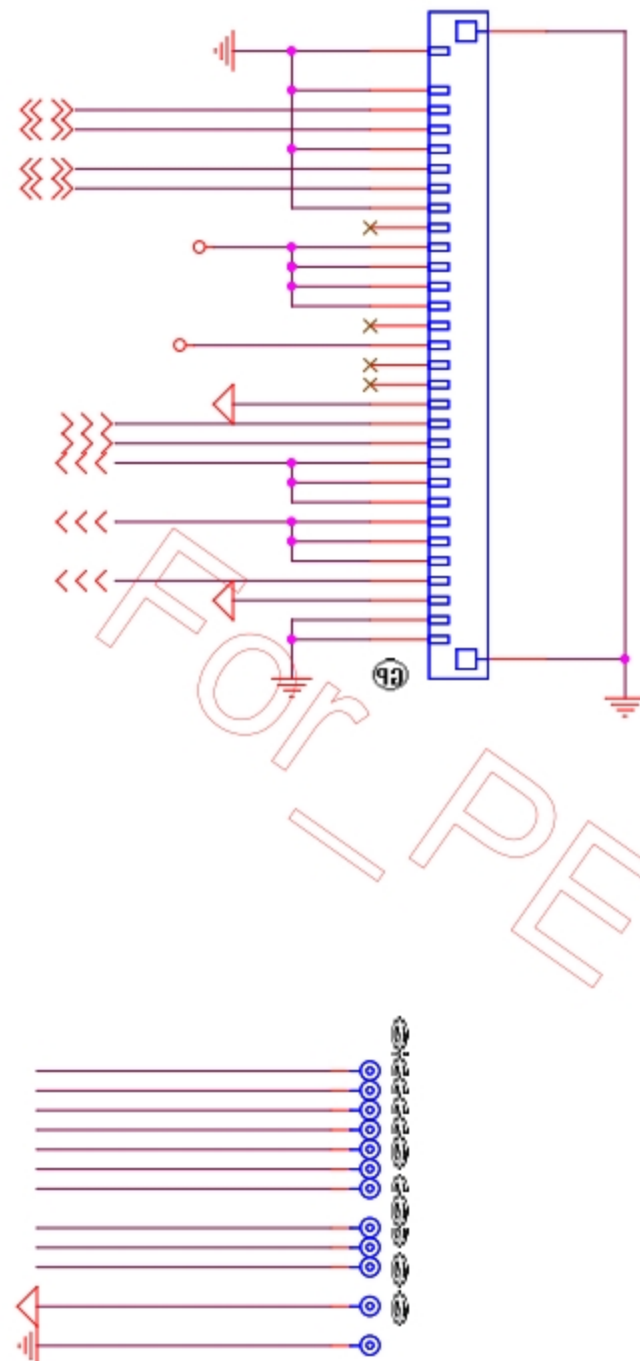


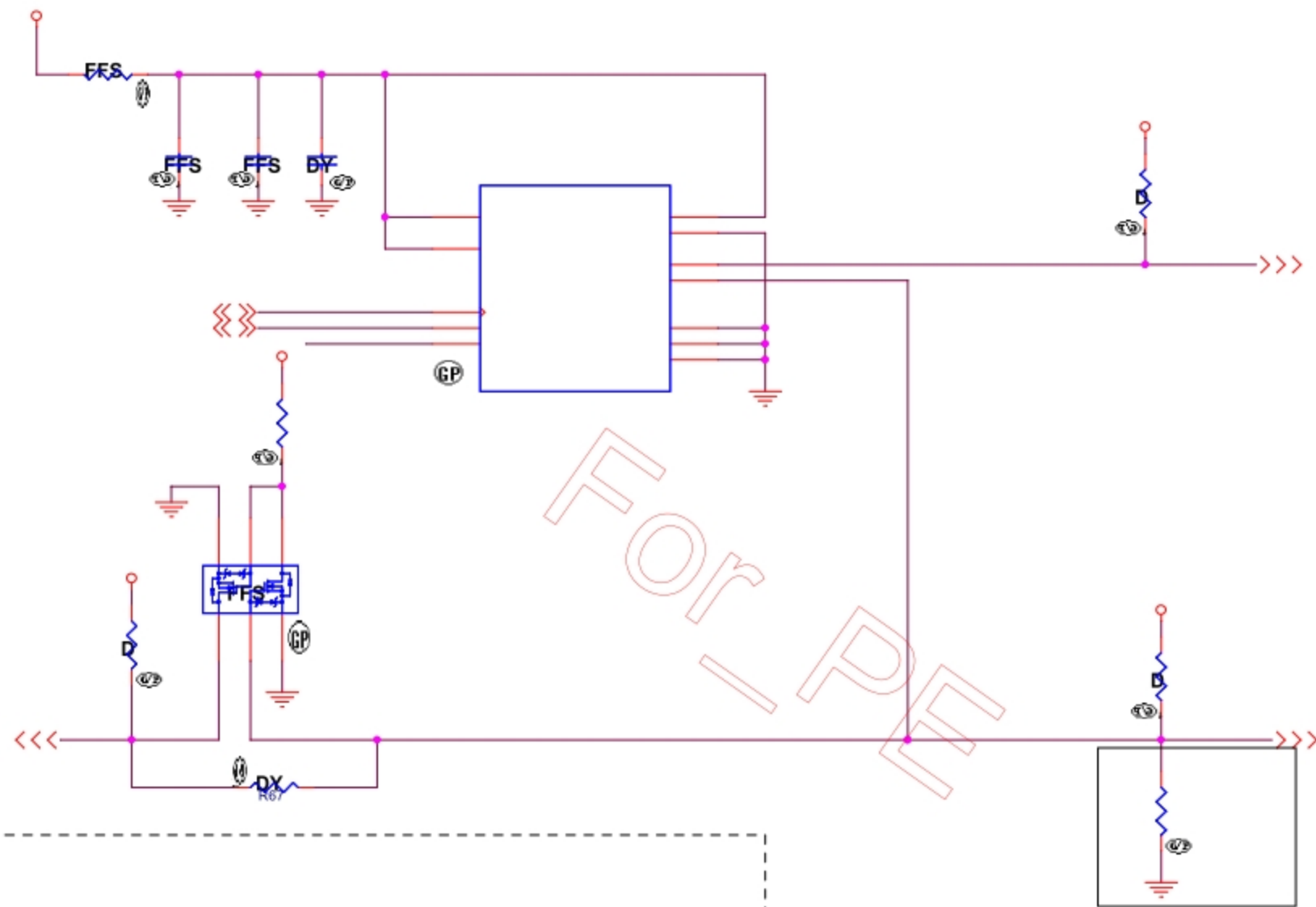

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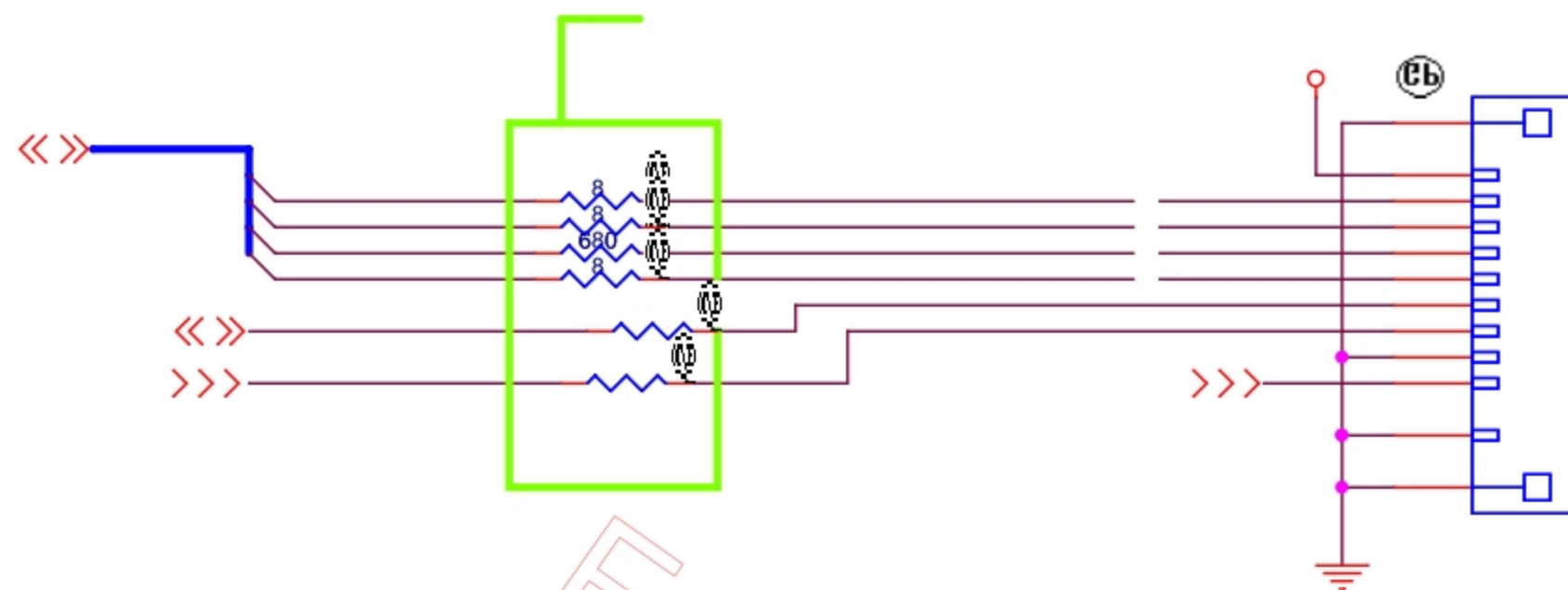
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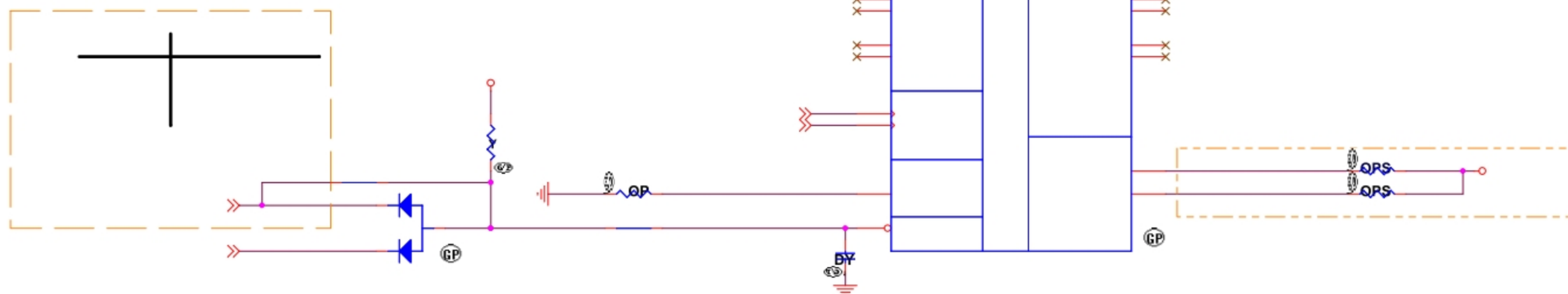
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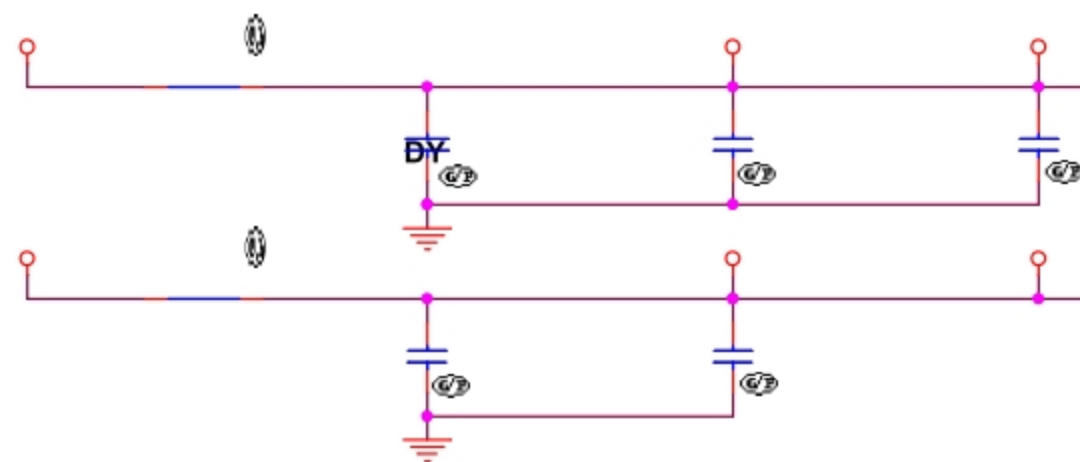
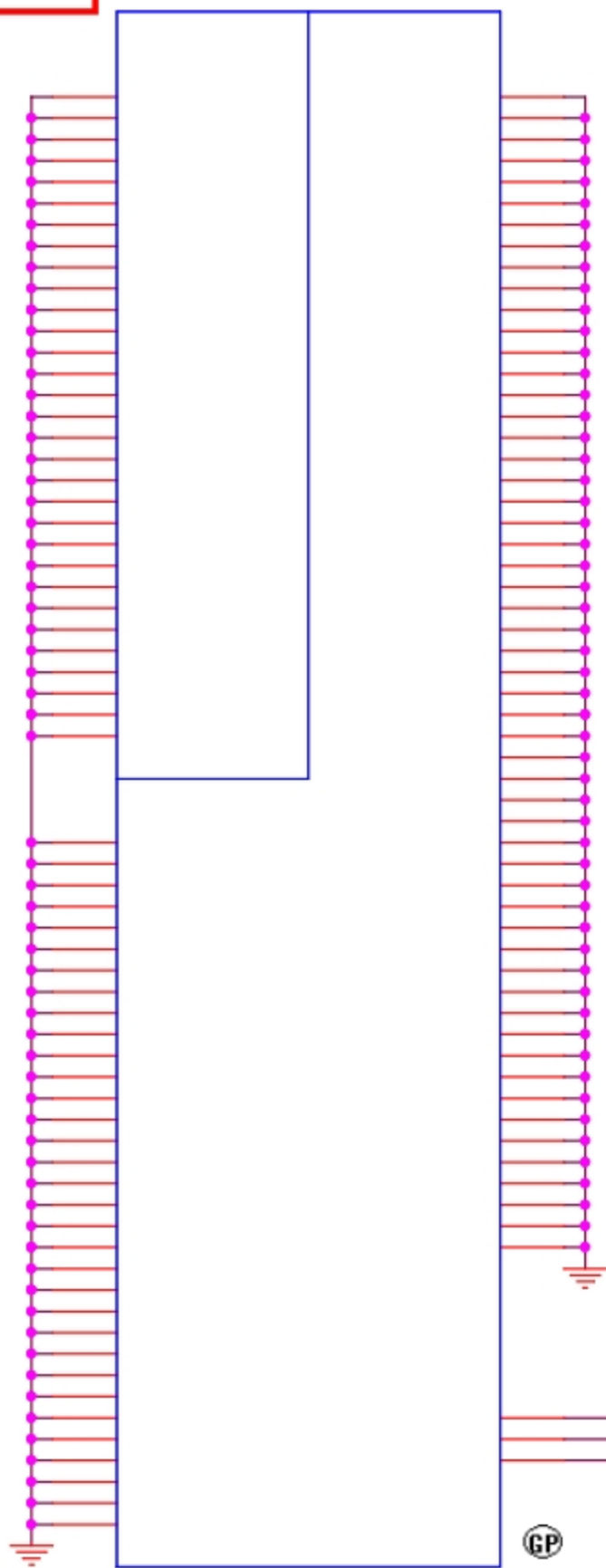
Table 3-5 PCI Express® Bus Interface

Pin Name	I/O	Description
PERSTb	I	Fundamental reset. 3.3-V tolerant pad.  This signal must be asserted during any fundamental reset event, such as power up, warm boot, reset button pressed, CTL-ALT-DEL, Windows restart, or wake from D3.
PCIE_REFCLKP/N	I	PCI Express PLL differential reference clock (+/-). 100-MHz (+ 300 ppm) input frequency; 0-V to 0.7-V single-ended swing.
PCIE_TX[7:0]P/N	O	PCI Express transmitter output data channel TX[7:0] (+/-). Differential serial data transmitted up to a 8.0-GT/s bit rate.
PCIE_RX[7:0]P/N	I	PCI Express receiver input data channel RX[7:0] (+/-). Differential serial data received up to a 8.0-GT/s bit rate.
PCIE_CALR_RX	I	Connect to PCIE_VDDC through a 1-k $\Omega$ (1% tolerance) resistor.
PCIE_CALR_TX	I	Connect to PCIE_VDDC through a 1.68-k $\Omega$ (1% tolerance) resistor.
CLKREQB	O	Reserved, do not connect on the PCB.

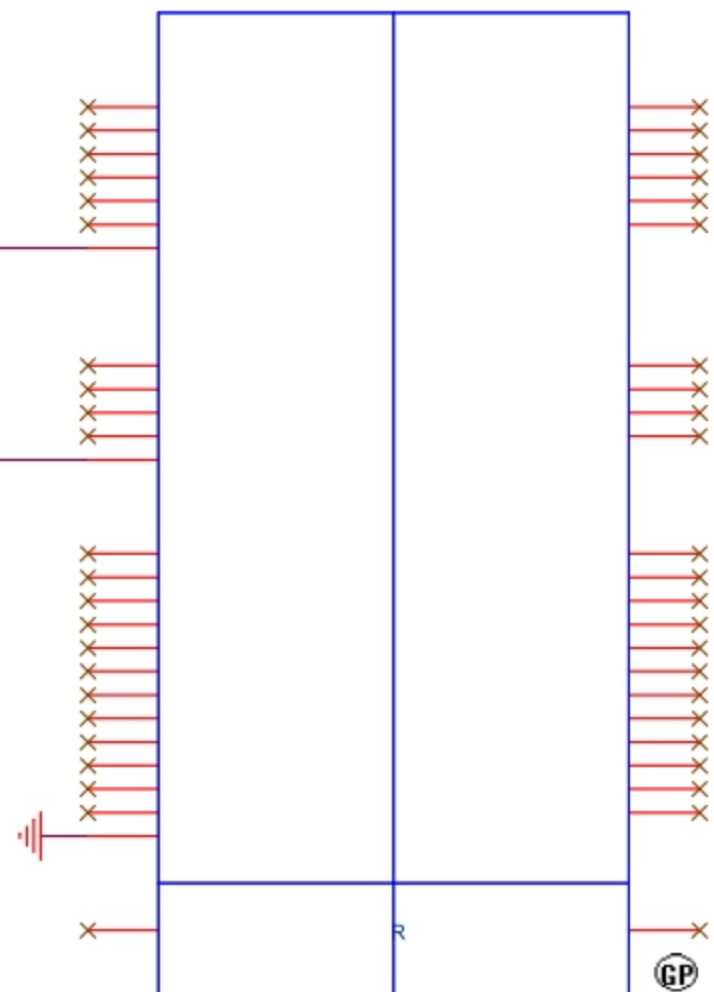
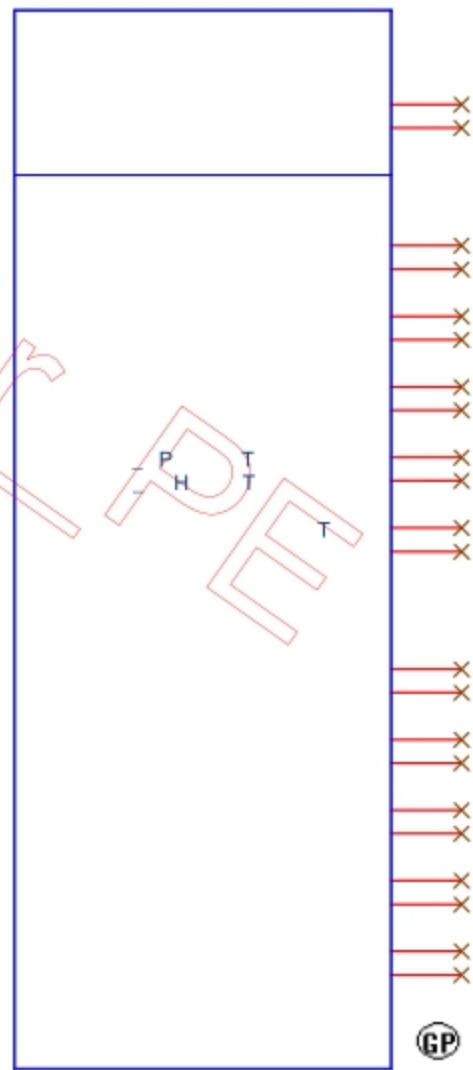


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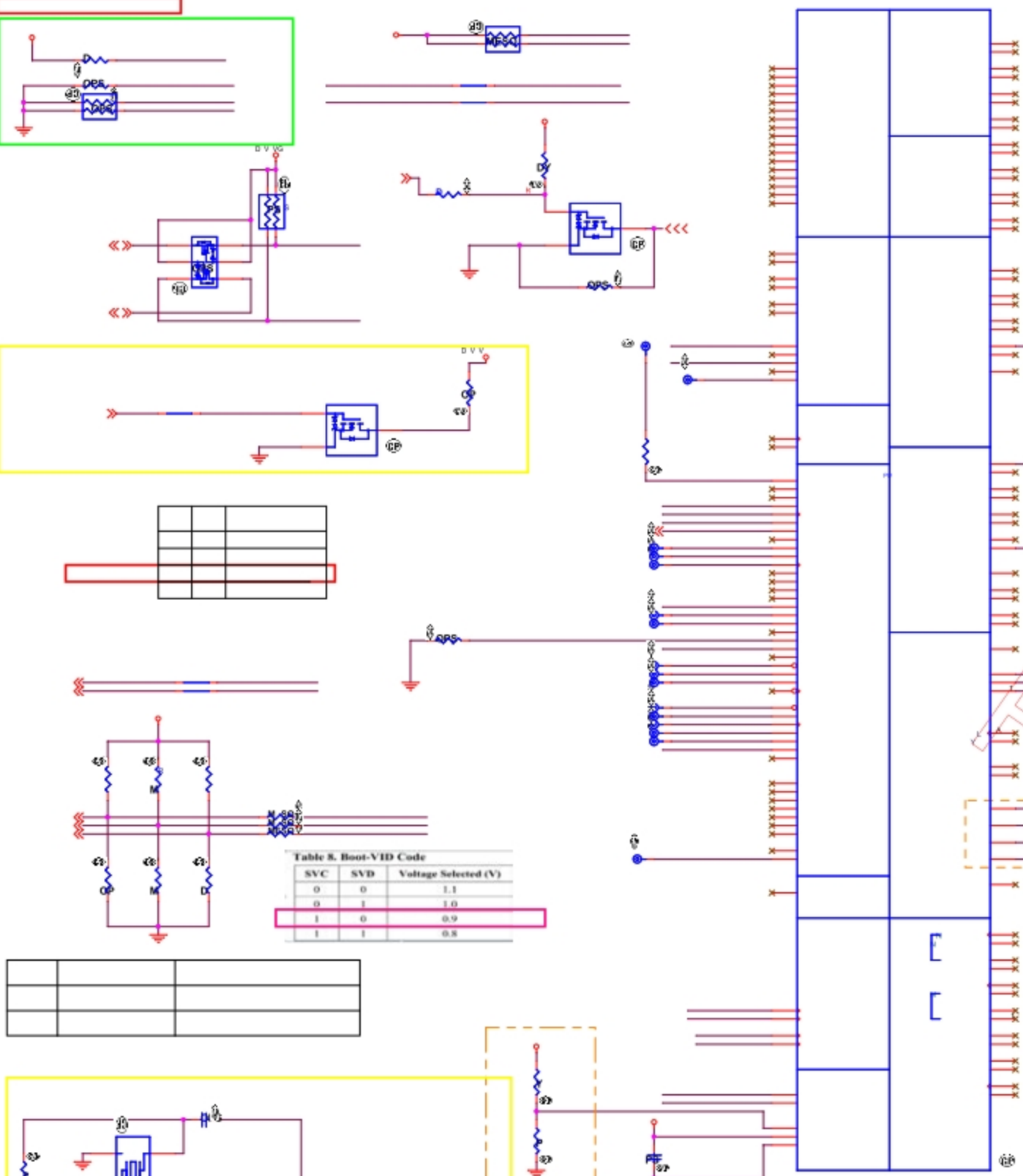


Table 8. Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

PS\_0

R_pu	R_pd	Bits(3:1)	Size of the Prima
NC	4750	000	128 MB
8450	2000	001	256 MB
4550	2000	010	512 MB
6980	4990	011	Reserved
4530	4990	100	N/A
3240	5620	101	N/A
3400	10000	110	N/A
4750	NC	111	N/A

PS\_1

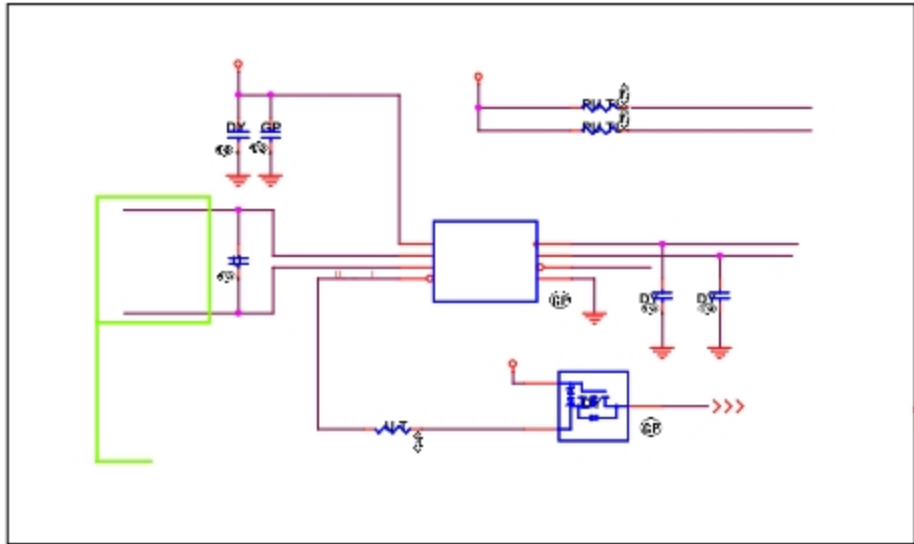
R_pu	R_pd	Bits(3:1)	Size of the Prima
NC	4750	000	128 MB
8450	2000	001	256 MB
4550	2000	010	512 MB
6980	4990	011	Reserved
4530	4990	100	N/A
3240	5620	101	N/A
3400	10000	110	N/A
4750	NC	111	N/A

PS\_2

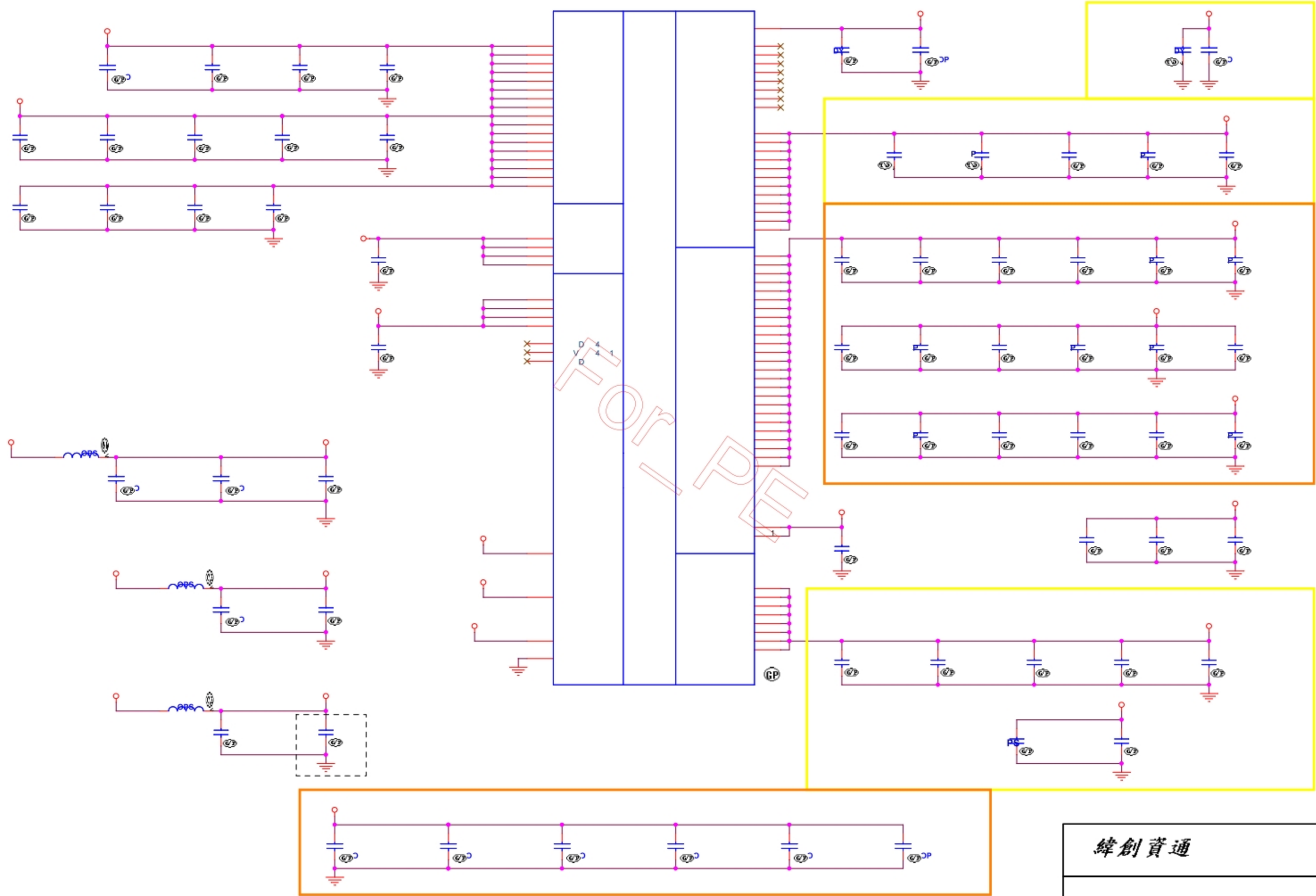
R_pu	R_pd	Bits(3:1)	Size of the Prima
NC	4750	000	128 MB
8450	2000	001	256 MB
4550	2000	010	512 MB
6980	4990	011	Reserved
4530	4990	100	N/A
3240	5620	101	N/A
3400	10000	110	N/A
4750	NC	111	N/A

MLPS Memory ID setting:

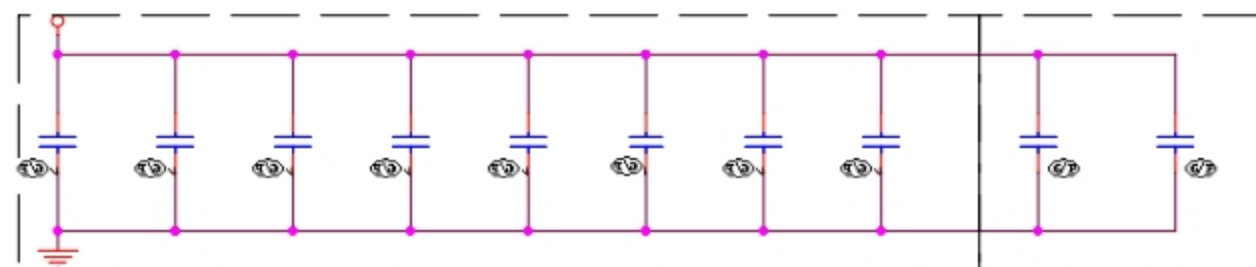
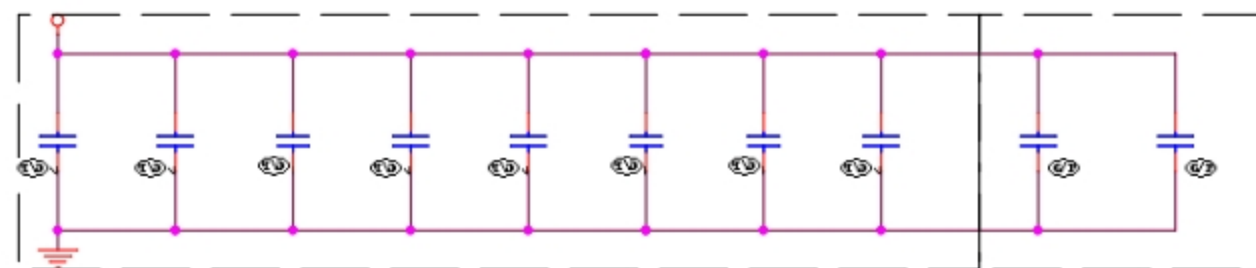
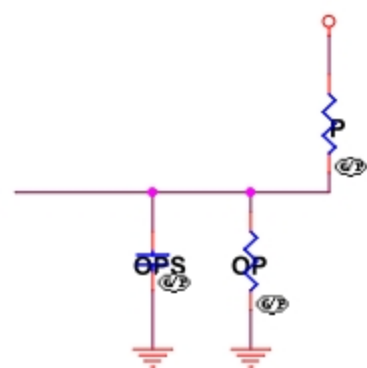
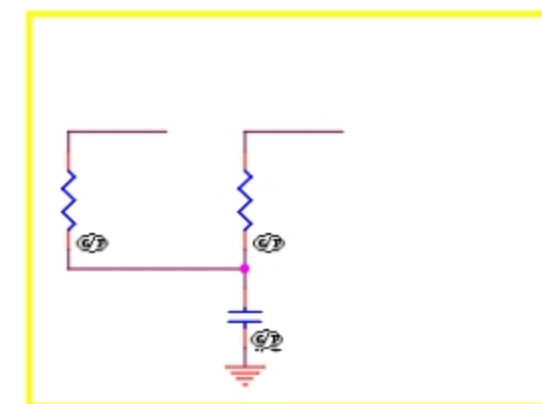
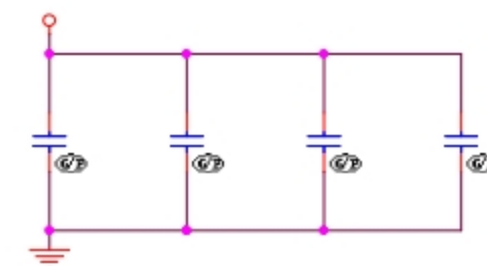
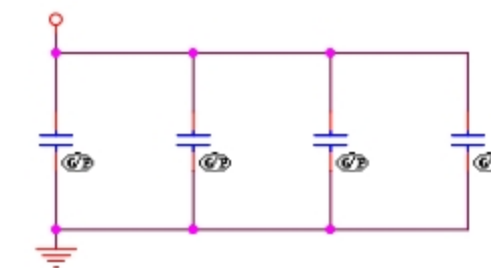
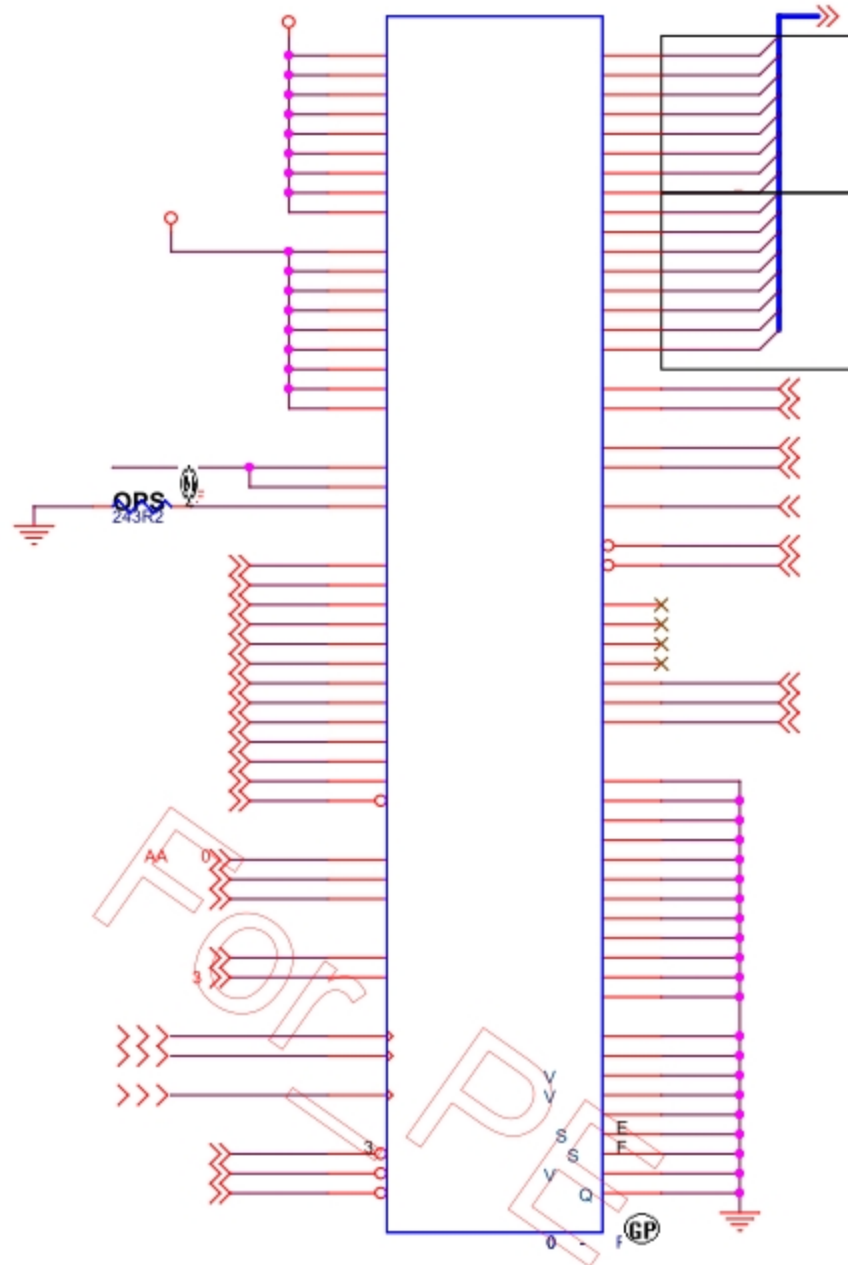
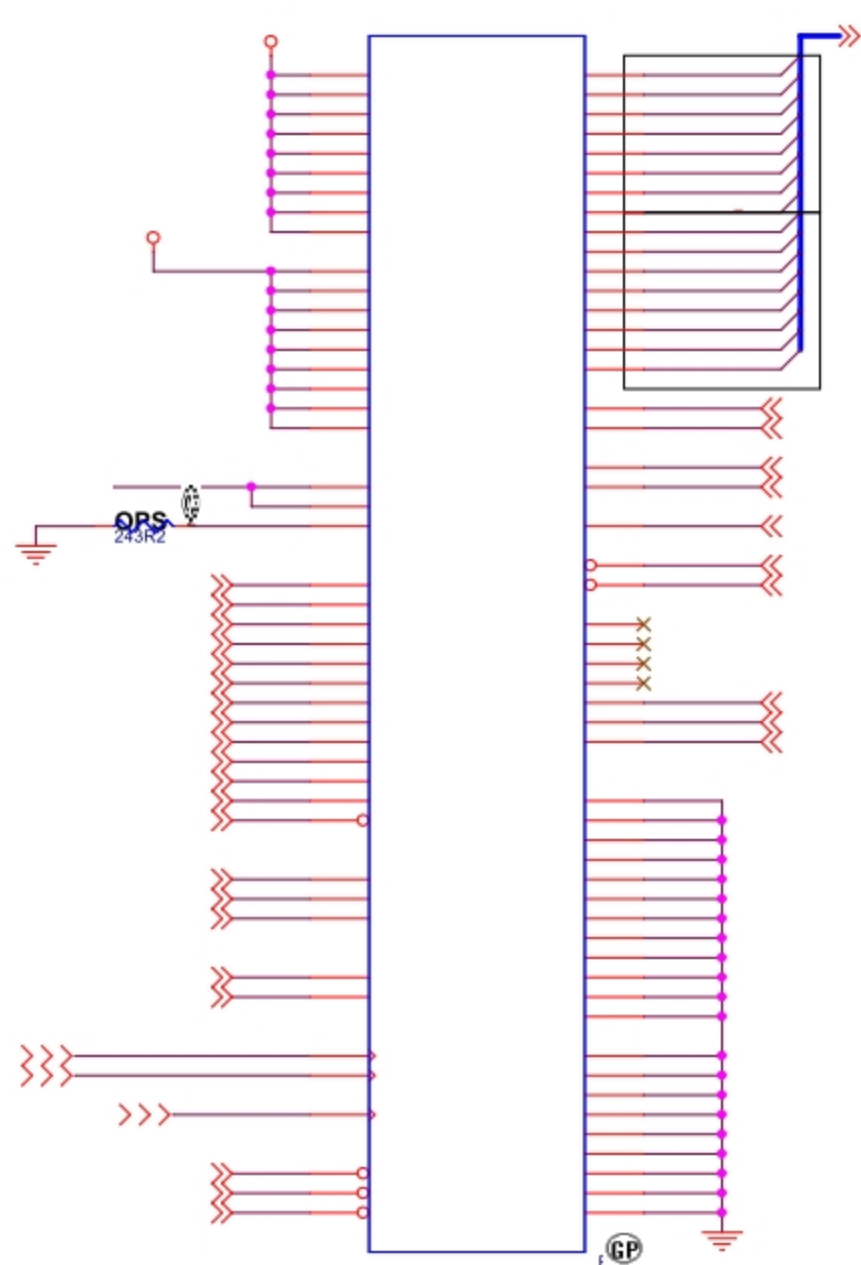
ID	[2:0]	Memory Type	Configuration	Row x Col x Bank bits	Channel Size	Vendor Pin	SMT quantity	R_pu	R_pd
0	000	Samung - DDR3L	256M x 16	200	2GB	K9W4G1E40E-DC1A	4 pcs	NC	4750
1	001	Micro - DDR3L	256M x 16	200	2GB	MT41J256M16LY-091G N	4 pcs	8450	2000
2	010	SK hynix - DDR3L	256M x 16	200	2GB	H5TC4G62EFR-N0C	4 pcs	4550	2000
3	011								
4	100								
5	101								
6	110								
7	111								



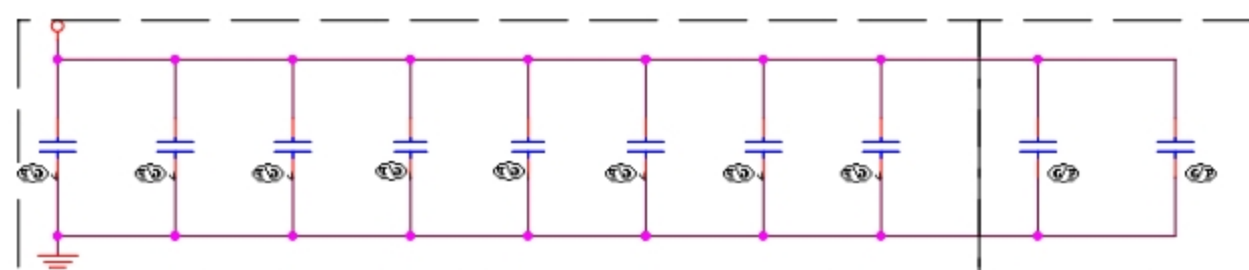
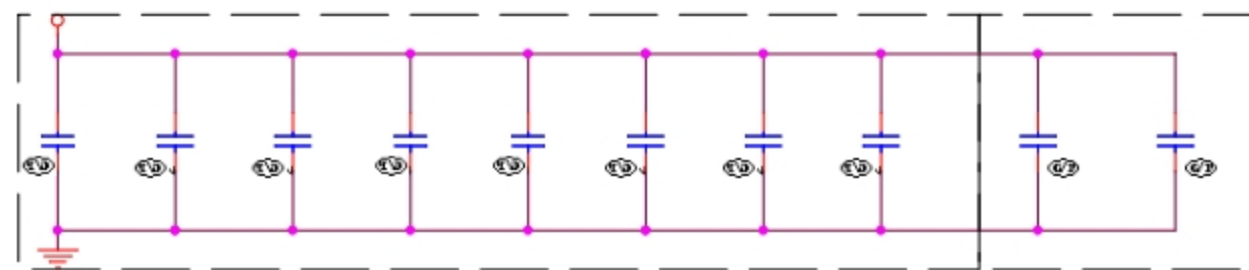
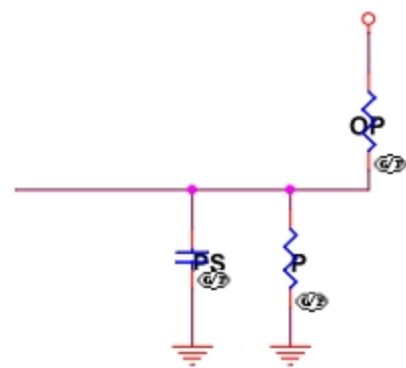
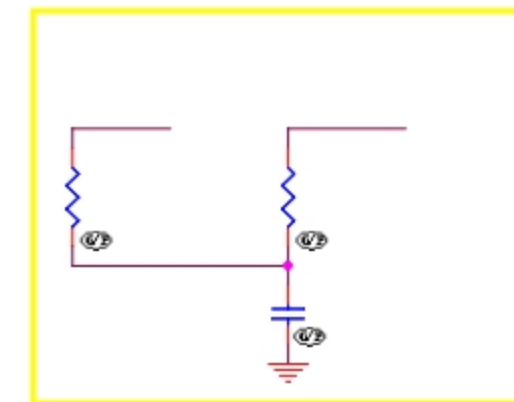
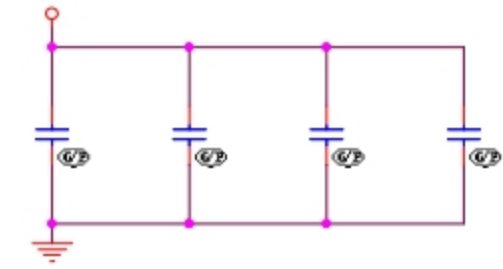
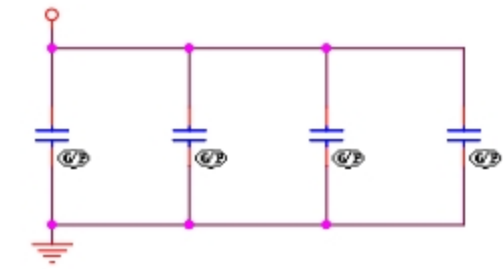
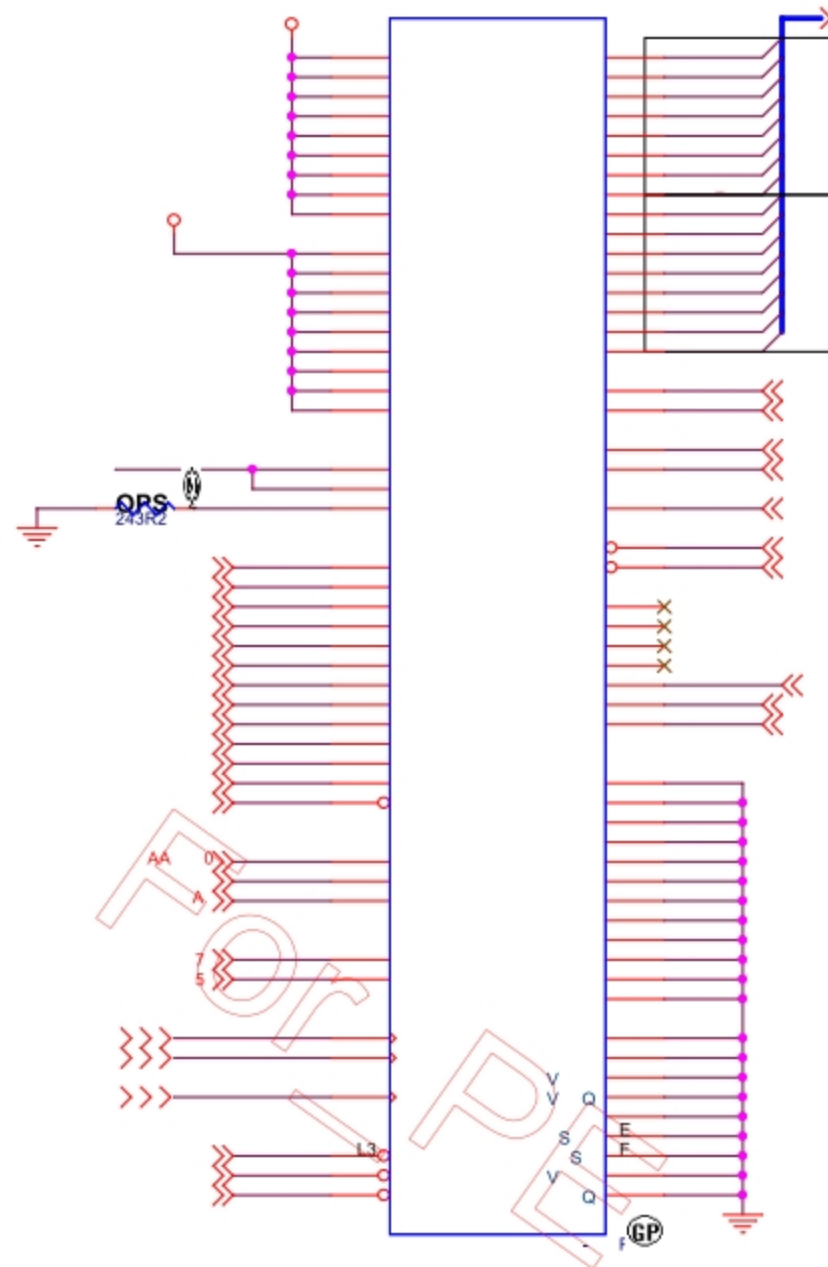
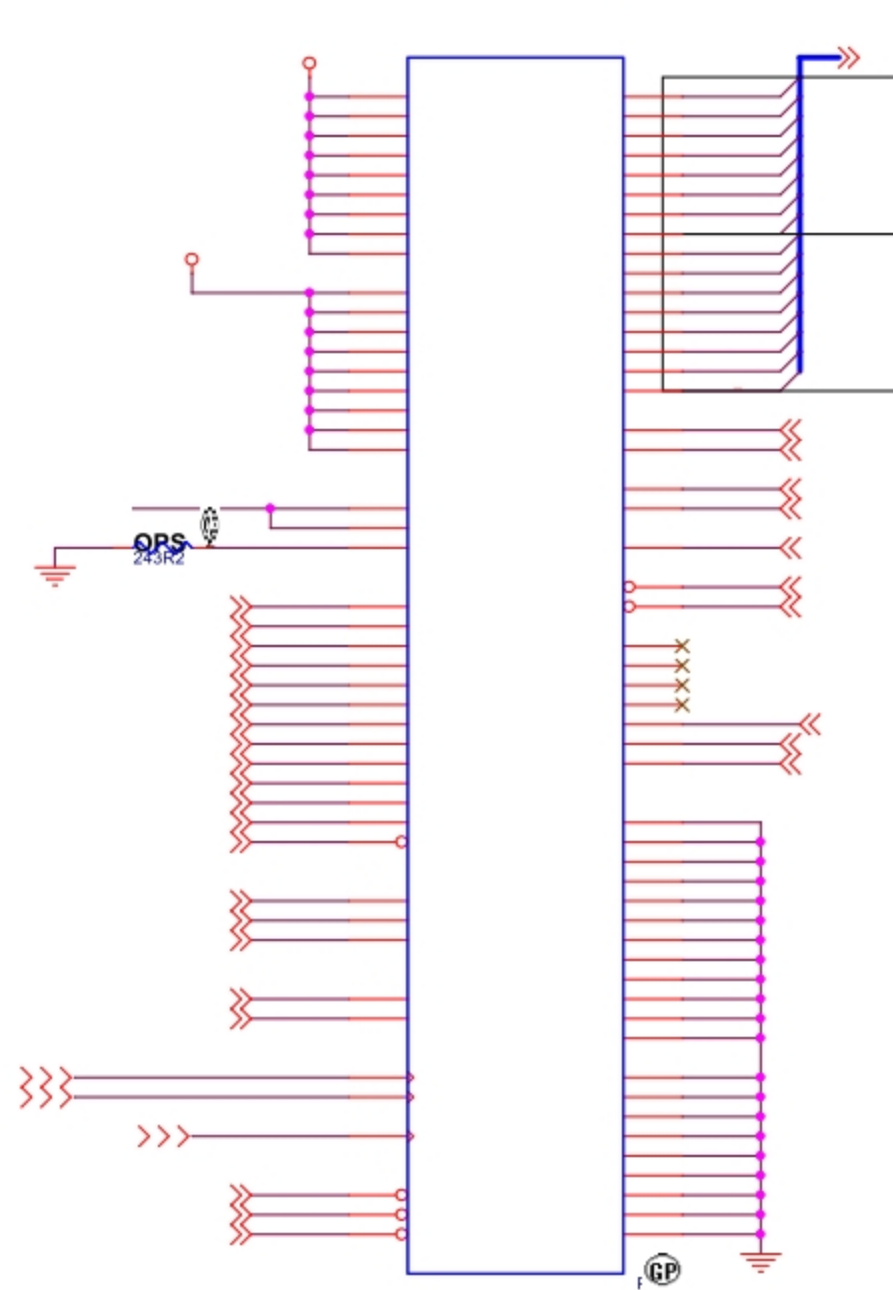
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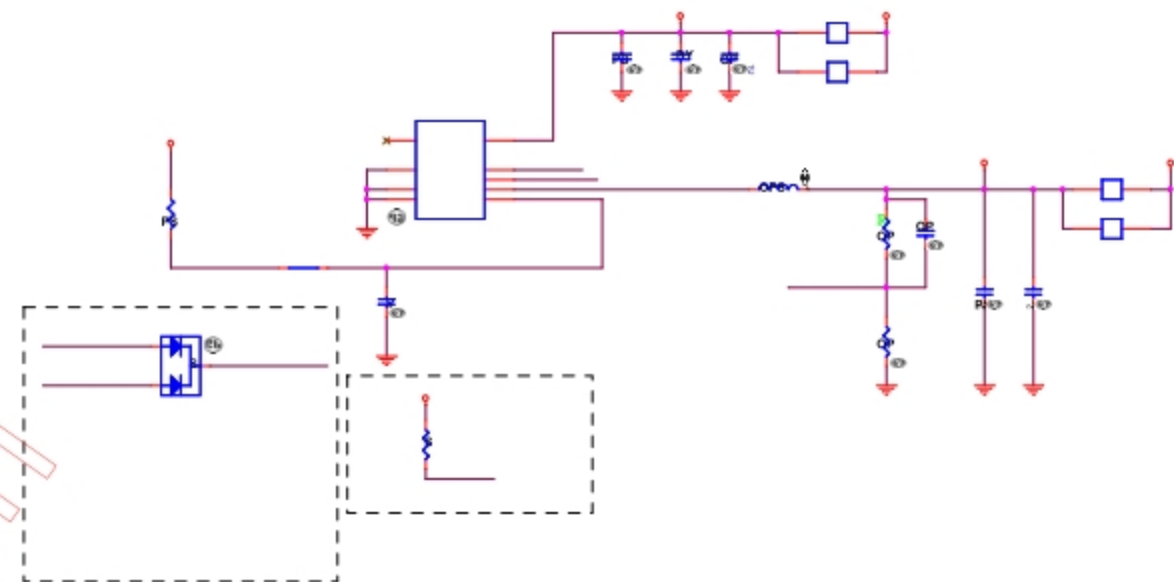
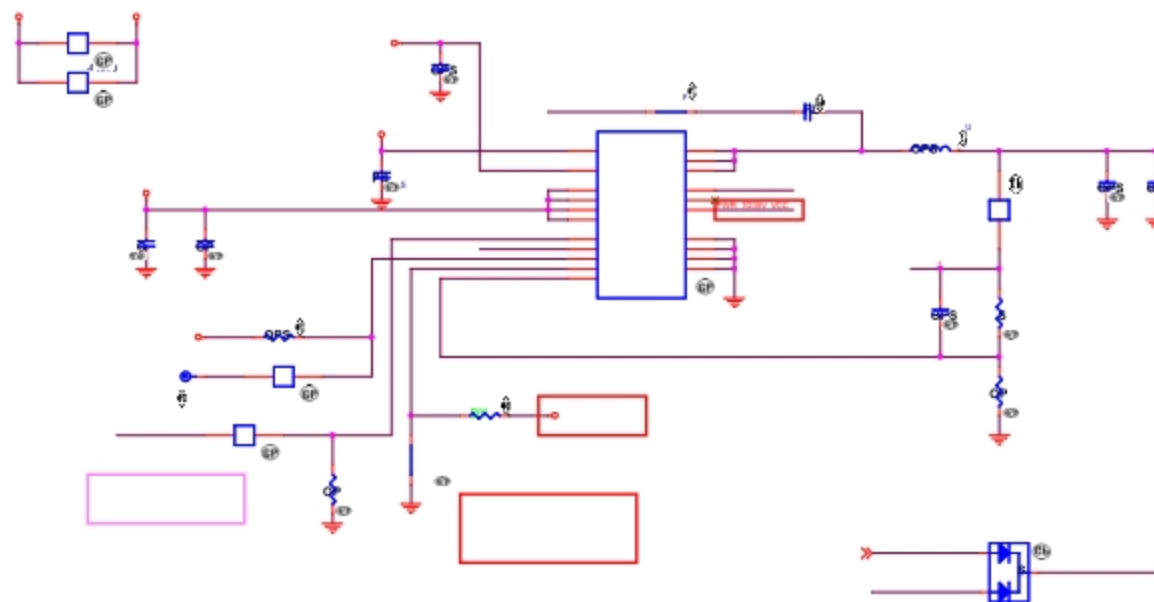
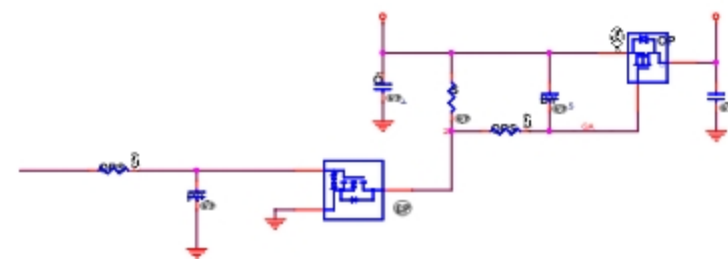
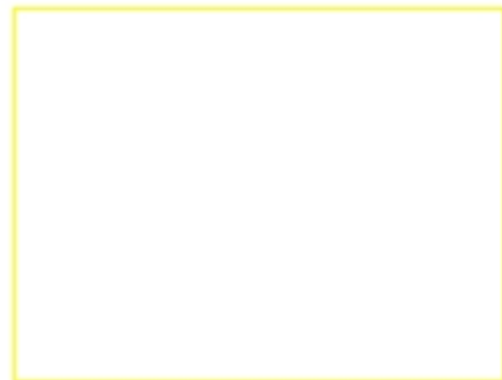
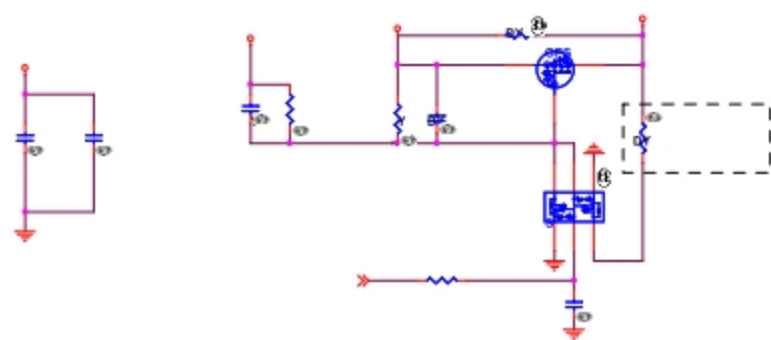
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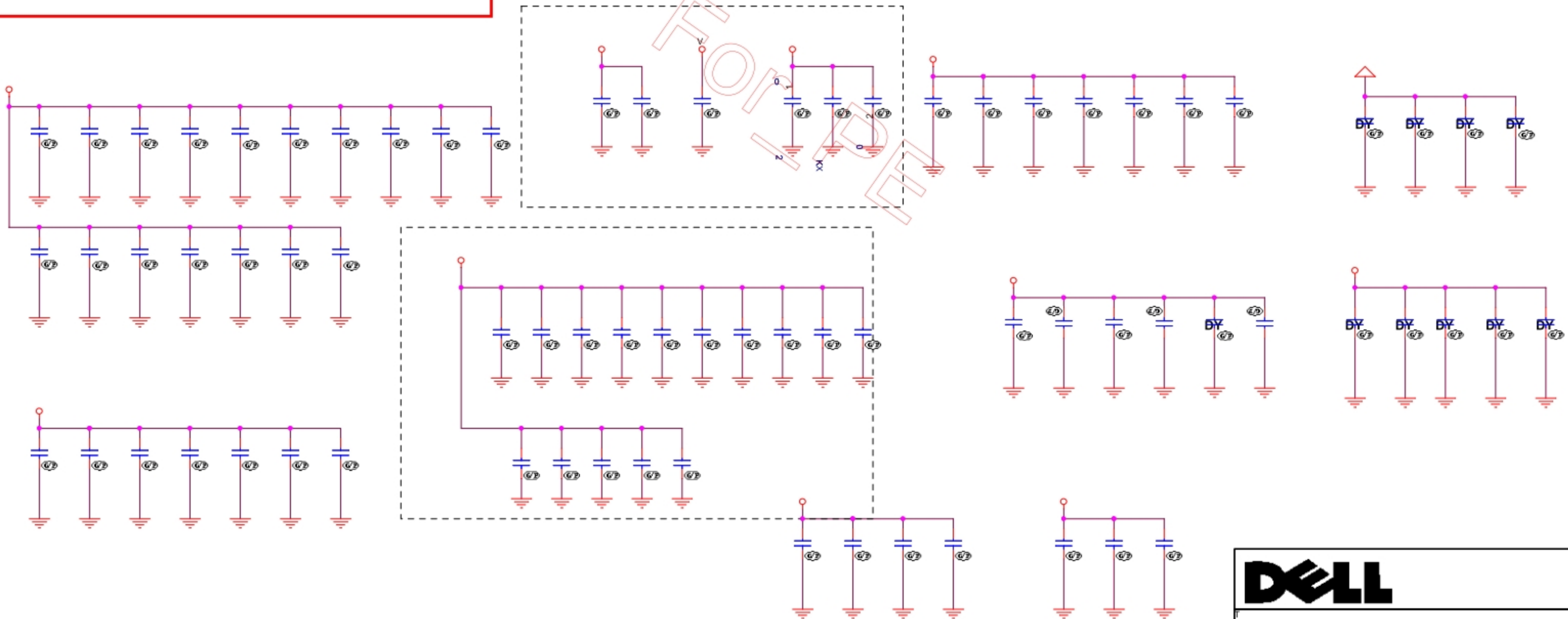
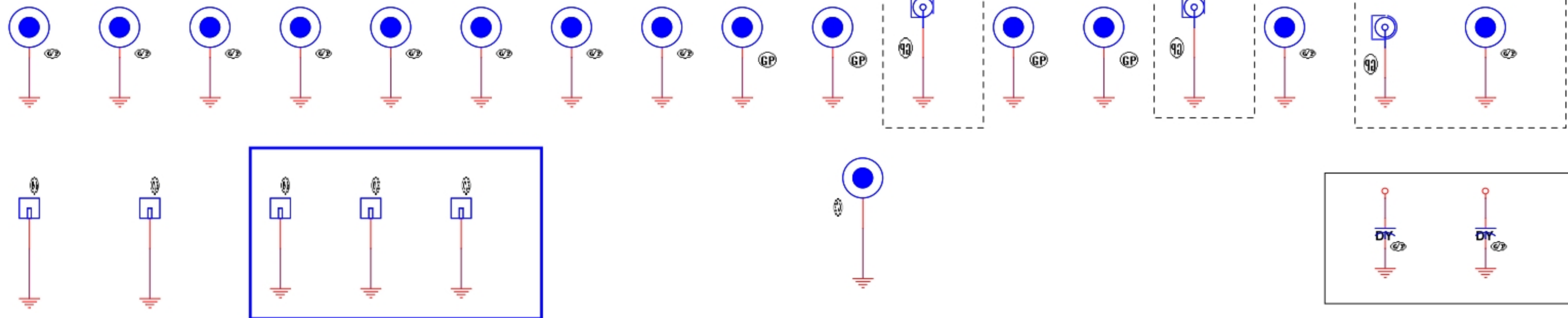


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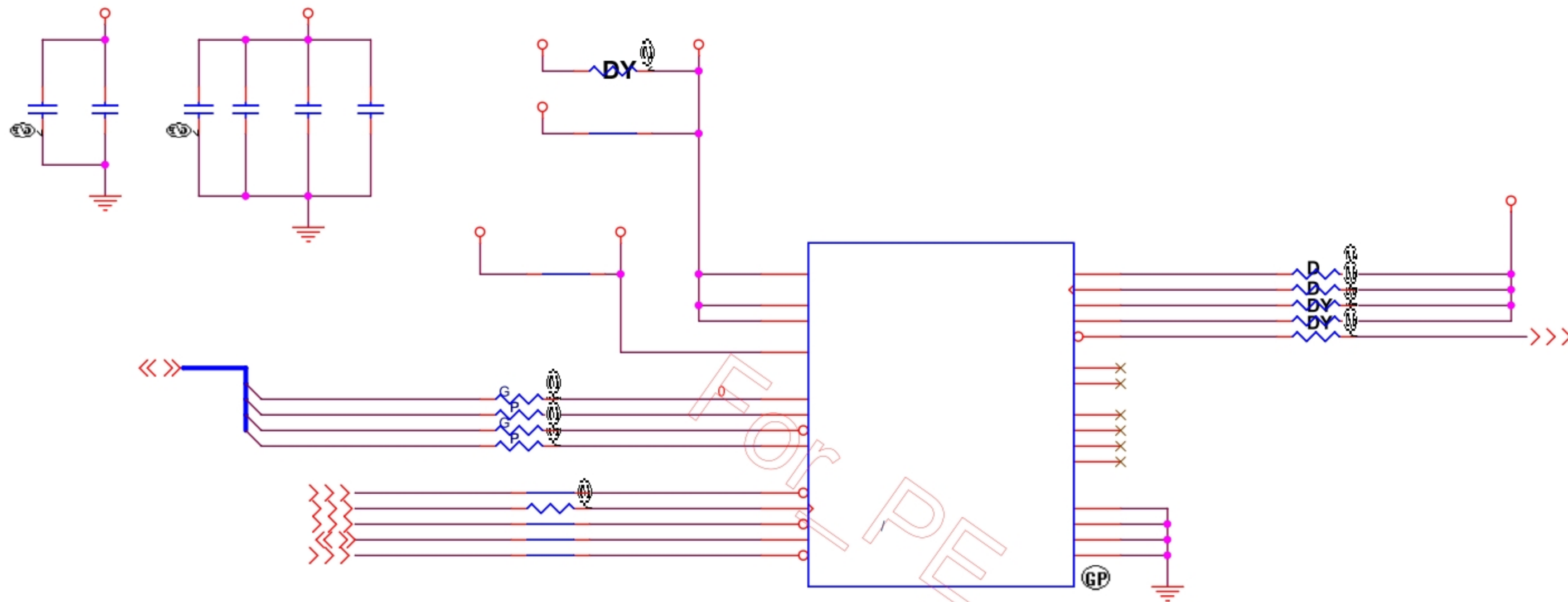
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### 1.6.2 LPC Host Interface

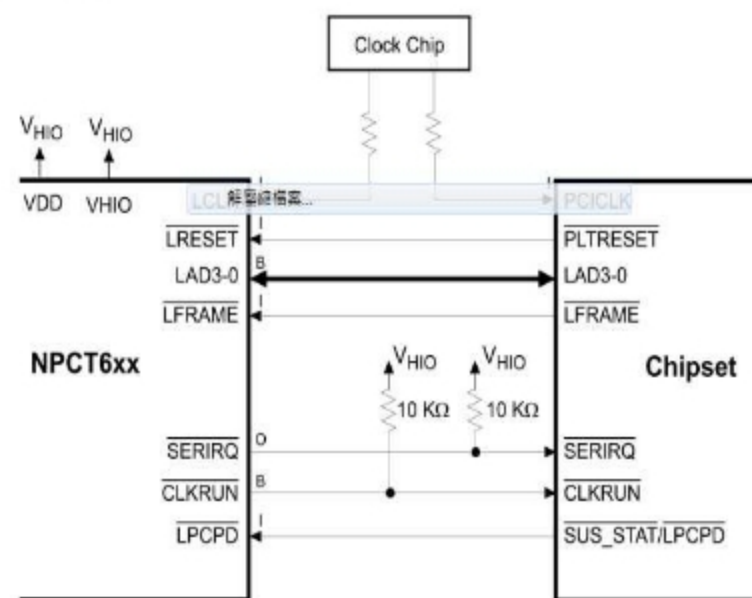
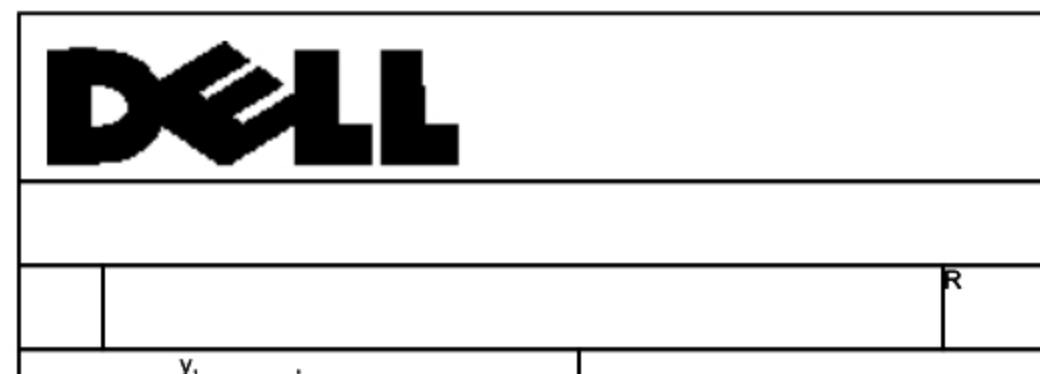
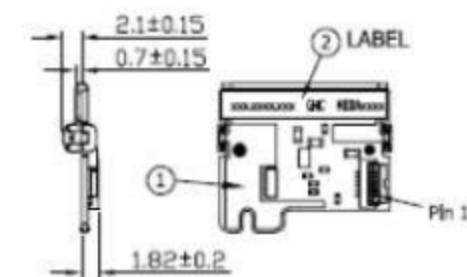
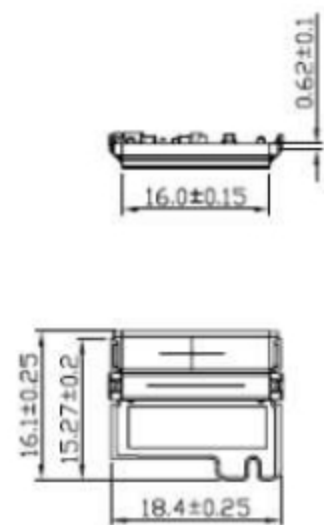
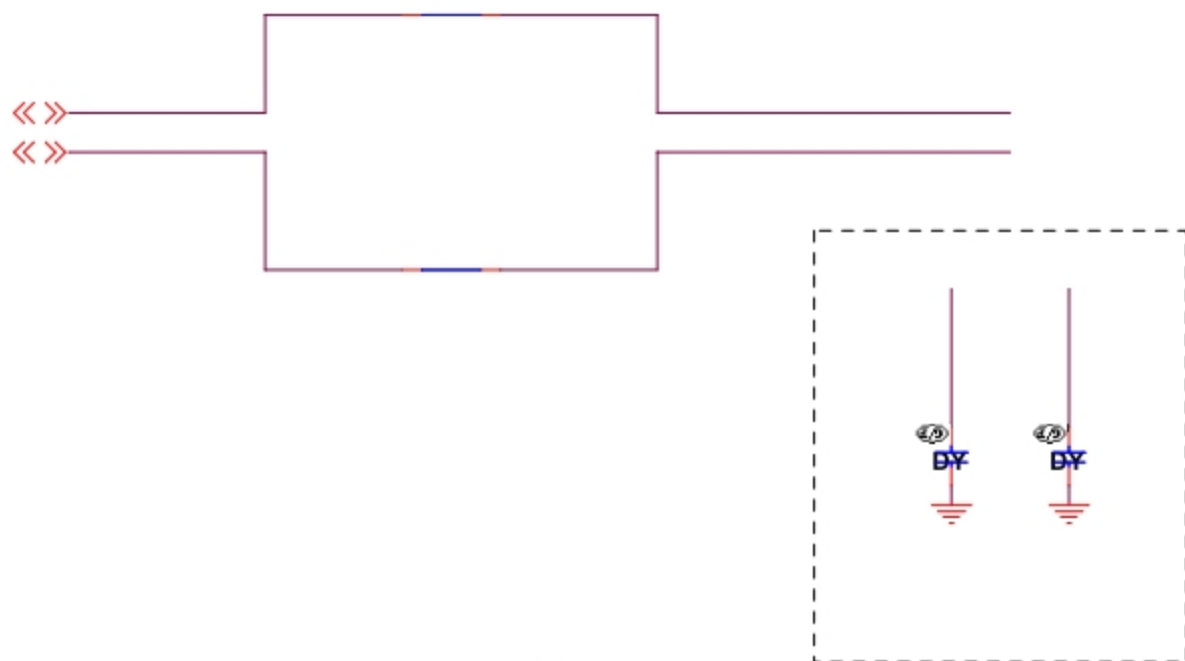


Figure 1-6. Host-LPC Interface Connection



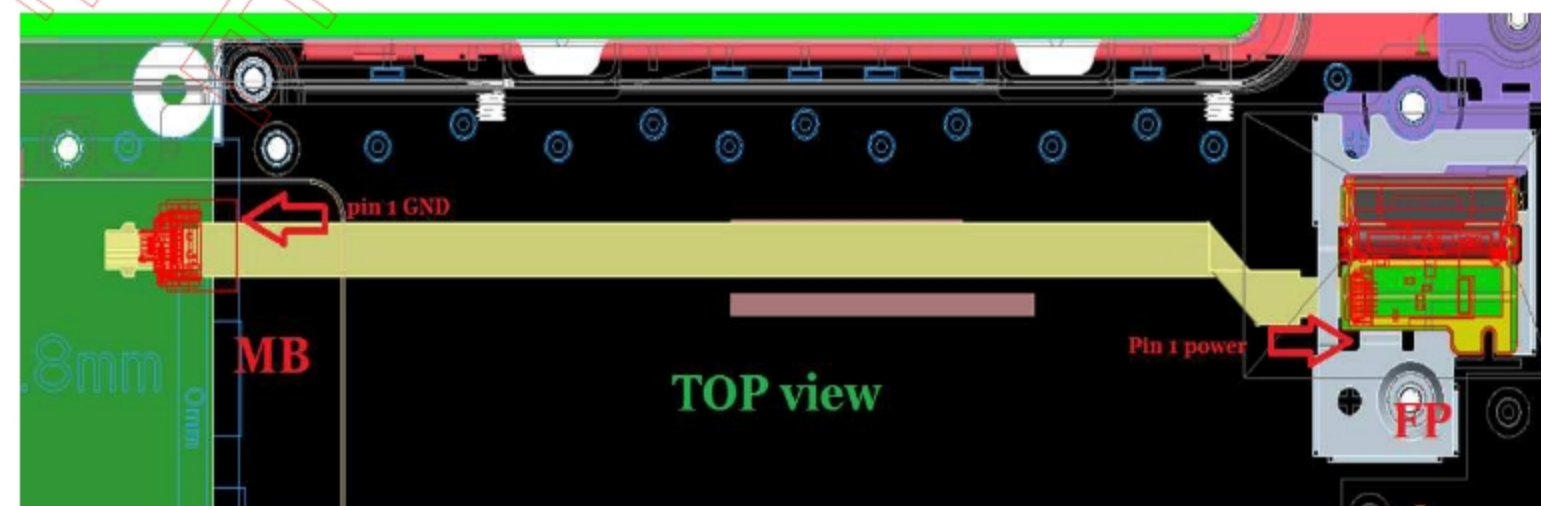


#### FingerPrint Pin Assignments.

- Pin 1 = 3.3V<sub>in</sub>
- Pin 2 = (ND)
- Pin 3 = D-
- Pin 4 = D+
- Pin 5 = Reset\_N
- Pin 6 = GND

Note :  
Module:

- 1.Sensor Type:Semiconductor
- 2.Interface:USB 1.0 and 2.0 Full Speed



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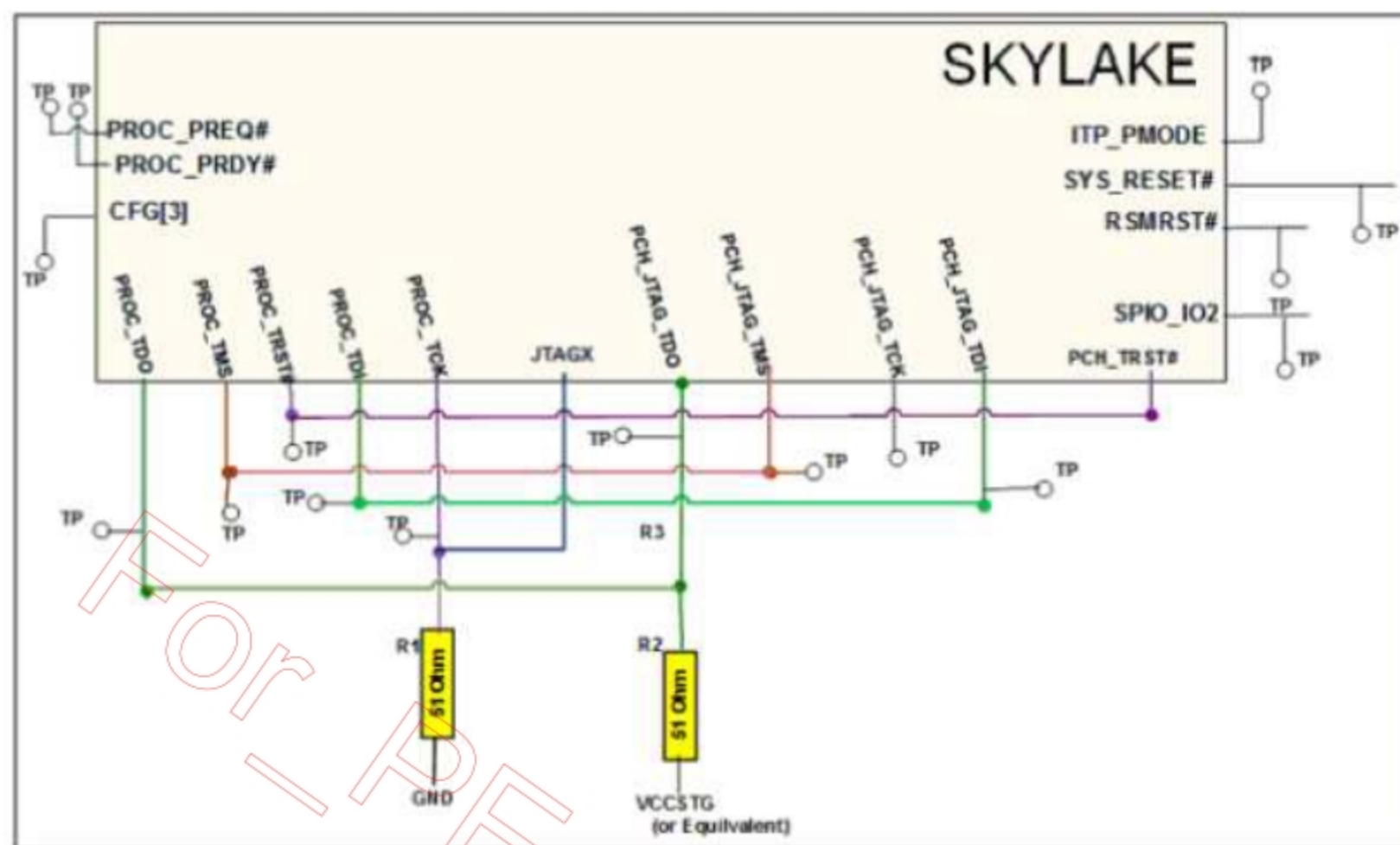
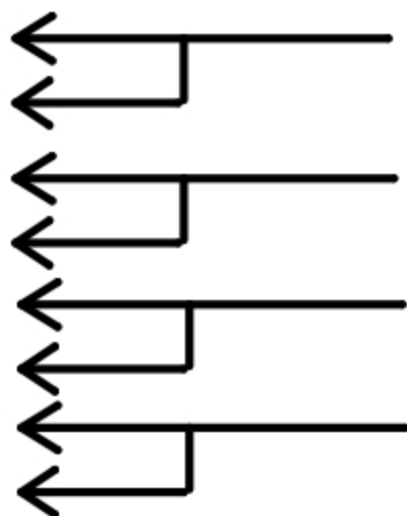
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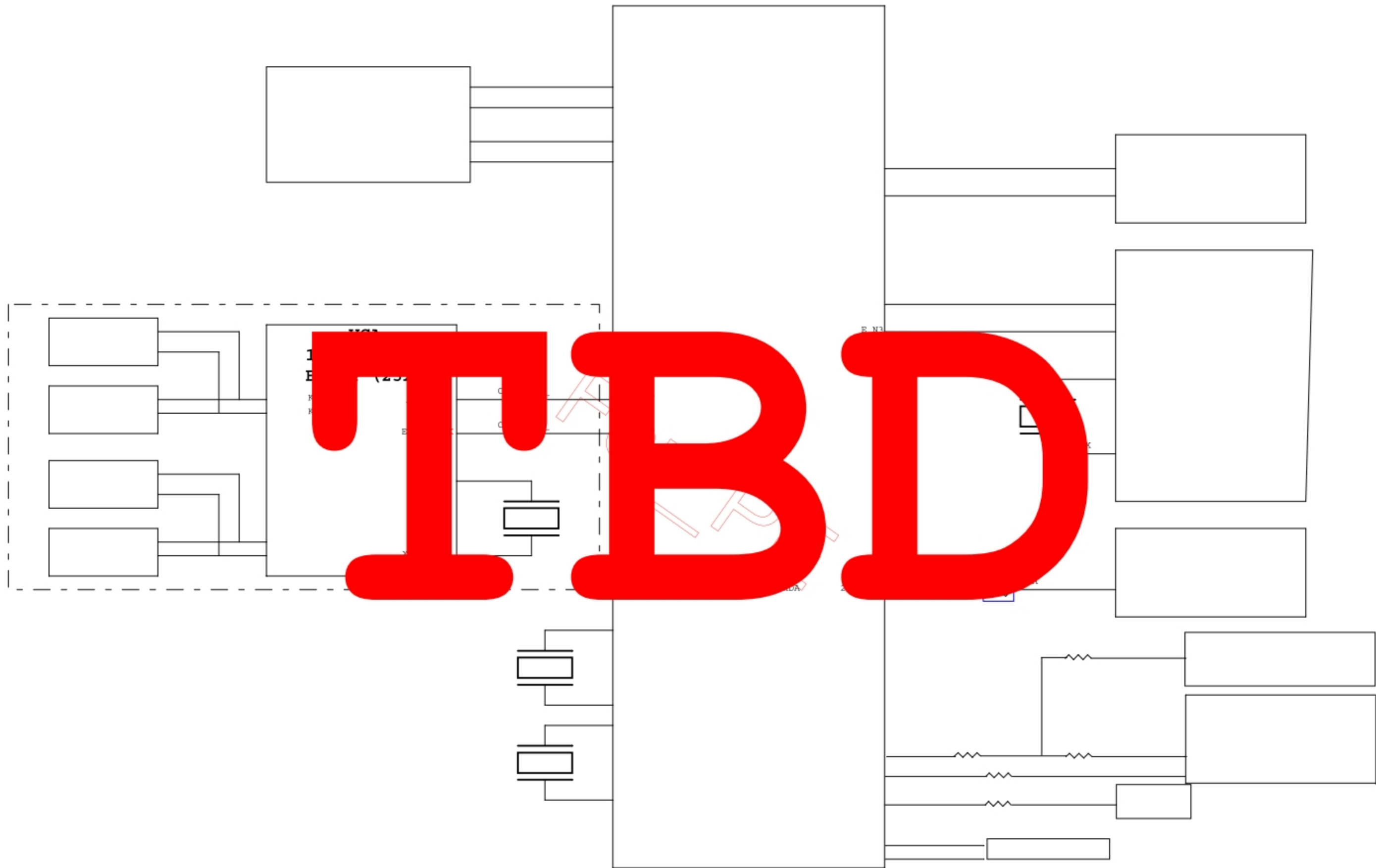
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